

Low Temperature Hybrid Bonding for Die to Wafer Stacking Applications

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Abstract— The direct bond interconnect (DBI®) technology is a platform technology that offers a hermetically sealed hybrid bond with solid metal-metal (Cu-Cu is the most common) interconnect at a relatively low thermal budget. The Xperi wafer to wafer hybrid bonding technology has been in high volume production since 2015. The Xperi die to wafer hybrid bonding technology, DBI® Ultra, is now ready for industry adoption and ramp to manufacturing. The bond takes place at room temperature in an ambient environment in a class 1000 cleanroom; therefore, offers bond throughput comparable to mass reflow flip chip assembly. A low temperature batch anneal after bonding results in a solid Cu-Cu connection surrounded by dielectric for improved thermal performance.

The value of the hybrid bonded Cu-Cu technology may be realized at various interconnect pitches for different applications. For die to wafer and die to die application with through silicon vias (TSVs), significant performance and cost advantages can be achieved at sub-40um pitch through elimination of both the solder and underfill materials from the package. Additionally, the technology may be scaled to sub-micron interconnects to enable widespread disaggregation and chiplet architecture innovation.

Xperi's development efforts target the sub-40um pitch die-to-wafer stacking, which can be enabled with the existing Si supply chain. Previously, we have reported assembly results with daisy chain die in single layer and in die-to-wafer stacking with or without TSVs.

In this paper, we report on a 5-die stack hybrid bonded module with TSV and the latest fabrication, assembly process, electrical

testing and reliability performance. The reliability tests include autoclave, high temperature storage and temperature cycling with pre-conditioning at MSL3 per JEDEC specification.

Keywords— low temperature Cu to Cu direct bonding, direct bond interconnect (DBI), DBI Ultra, hybrid bonding, TSV integration, D2W, D2D, stacking, reliability

I. INTRODUCTION

Direct Bond Interconnect (DBI®), a low temperature hybrid bonding technology [1, 2, 3], was first demonstrated by Ziptronix in a die-to-wafer (D2W) bonding format. However, for the first high volume manufacturing product was wafer-to-wafer (W2W) application. In 2015, Sony adopted the technology for CMOS image sensors [4]. Since then, development work has focused on high volume manufacturing of die-to-wafer hybrid bonding technology to enable enhanced performance in electronic products.

Current high throughput die bonding equipment alignment capability is $\sim 3\mu\text{m } 3\sigma$, which translates into a bonding pitch of 30 μm or larger for volume manufacturing and is well aligned for numerous die attach assembly products today.

Steady progress in die to wafer hybrid bonding has focused on single die to wafer assembly and reliability then die stacking [5, 6, 7, 8, 9, 10, 11]. Previously the daisy chain test die had a similar size to a high bandwidth dynamic random-access memory (HBM DRAM) die, 8 mm x 12 mm. The longest daisy chain structure had 31,356 links and covers an active area of 5.36mm x 9.36mm. In previous test vehicles the bonding pitch

ranged from 10 to 40 μm with a pad diameter of either 5, 10 or 15 μm . We have demonstrated single layer bonding and achieved high electrical test yield and superior reliability in temperature cycling, high temperature storage and autoclave tests in these single die test vehicles with a face to face assembly[8].

After the initial success with die stacks with no TSV, we designed and fabricated a test vehicle with TSVs that allows electrical testing of all interfaces in a stacked die package with a similar x-y footprint. In 2020, we successfully demonstrated the integration of TSV into a 4-layer stacked package using this test vehicle[12, 13].

In this paper, we report the latest results in wafer and die fabrication, assembly process optimization, electrical testing and reliability testing on a 5-die stacked module with TSVs. The resistance of a daisy chain in the 5-die stacked modules are measured on stacked modules subjected to JEDEC standard tests commonly used for memory packages qualification, including autoclave, high temperature storage and temperature cycling tests with MSL3 pre-conditioning.

II. TEST VEHICLE DESIGN AND FABRICATION

Fig. 1 shows the schematic layout of Xperi's daisy chain test vehicle with TSVs. The die contains several features that mimic a DRAM HBM die including a central row of TSVs arrays and two TSV arrays at mid-radii between center and edge. The die size is 8 mm x 12 mm x 50 μm , and the TSVs are 5 μm diameter at a 35 μm pitch. The main array in the center region of the die and has 9,480 TSVs, more than double the TSV count of DRAM HBM2 packages on the market. The left and right array each has 632 TSVs and the left edge array has 2,528 TSVs. Five die stack modules were built with 4 TSV die and one top die to connect the TSVs and complete the test vehicle circuit. The longest daisy chain in the 5-die stack has over 47,000 interconnects. The probe pads for resistance measurement are on the host wafer.

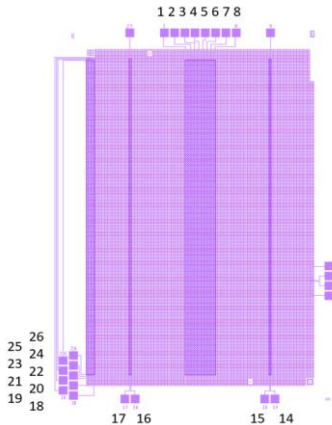


Fig. 1. Schematic of the TSV test vehicle. Dark purple areas represent TSV arrays

Fig. 2 shows a simplified process flow for the TSV die fabrication. The first two steps: fabrication of the TSV array

and the front side re-distribution layer (RDL) are completed by our partner at Fraunhofer Institute for Reliability and Micro-Integration, IZM – ASSID in Dresden, Germany. The direct bond pads and the remaining process steps are completed at Xperi.

The process flow is similar to the flow for fabrication of a TSV die with solder micro bumps, but easier with fewer steps (Fig. 2). It includes completing BEOL process on the front side of the wafer to add the hybrid bond pads, temporary bonding to a carrier wafer, backside wafer thinning, TSV reveal, TSV planarization, debond and sigulation. This process is compatible with existing packaging infrastructure in manufacturing today.

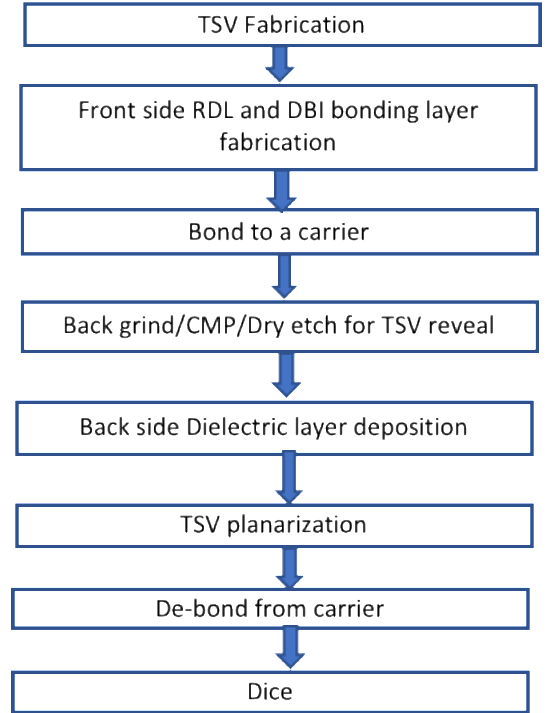


Fig. 2. Schematic process flow for fabrication of the daisy chain test die with TSV

Fig. 3 shows images of the test vehicle die front side (3a), back side (3c) and cross-section (3b) prior to bonding. The bond pad on the front is oversized to 15 μm to relax alignment accuracy requirement during bonding. The TSV diameter on the backside is 5 μm . The planarized TSV will be bonded directly to the DBI pads on the front side surface.

The host wafer for bonding has a complimentary RDL layer to enable formation of the daisy chain after bonding. The host wafer requires some specialized processing to prepare for reliability testing. The 5th die which completes the daisy chain is prepared in the cap wafer with a RDL layer and a DBI layer.

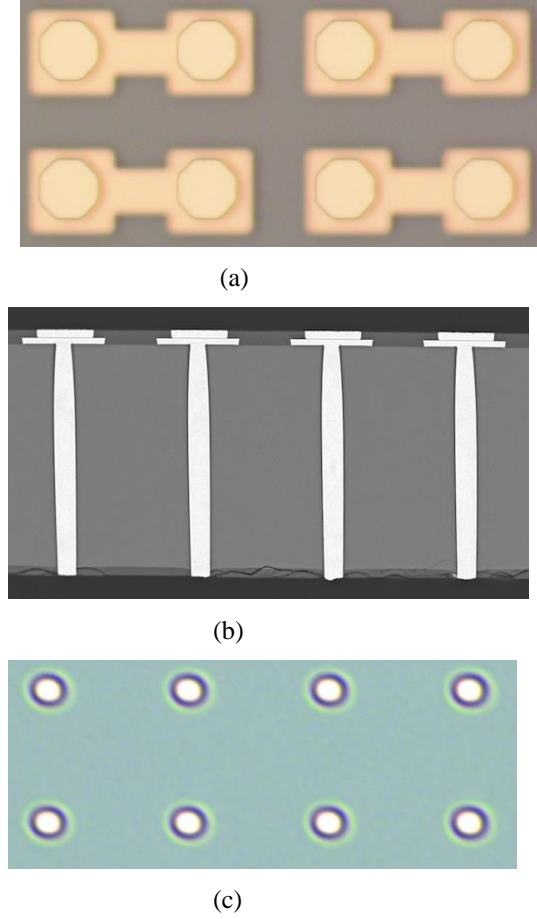


Fig. 3. The daisy chain test die with TSV: (a) Optical image of the front side DBI bonding pad and RDL layer for daisy chain connection; (b) SEM cross section image showing the front and back side bonding surfaces; (c) Optical image of the planarized TSV on the back side.

III. DIE AND HOST WAFER PREPARATION, ASSEMBLY AND TEST

A. Die and Host Wafer Processing Prior to Bonding

With the D2W hybrid bonding process we developed, all die processing prior to bonding is conducted with the die remaining on tape in a dicing frame. Die-on-tape handling is a standard within the packaging industry that minimizes damage of thin die and offers a low cost HVM solution for a wide variety of die sizes. The host wafer is rinsed and activated in plasma prior to bonding.

B. D2W Stacking

Bonding was carried out using a Datacon 8800 Chameo flip chip bonder with alignment capability of $3\ \mu\text{m}\ 3\sigma$. The $15\ \mu\text{m}$ pad on the front side surface shown in Fig. 3a was designed to meet the alignment accuracy of the pick and place bonder. Bond pads on the host wafer are also $15\ \mu\text{m}$ diameter. The bonding process is very similar to a flip chip pick and place process with no flux dip with similar throughput. Bonding takes place at ambient condition. When a die is placed on the wafer surface, spontaneous bonding of the oxide occurred. We stacked 4 layers of TSV die and a 5th cap die to complete the stacked module for electrical continuity.

After all 5 layers were bonded, the host wafer was annealed at $200\text{-}250^\circ\text{C}$ for 1 hour. Direct Cu-Cu bonding through the entire stack occurred in this single anneal process. The anneal temperature was held at $200\text{-}250^\circ\text{C}$ to ensure compatibility with temperature sensitive applications such as DRAM. The bond quality is characterized with C-mode scanning acoustic microscopy (CSAM) for bonding interface voiding, electrical resistance measurement for continuity, and cross-section microscopy analysis for quality of the Cu-Cu bonding interface.

C. Assembly Yield

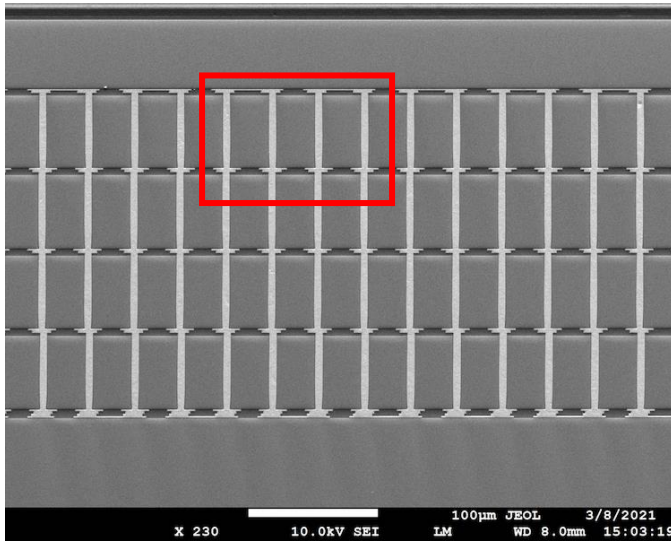
As reported in prior publications [12, 13], we achieved $>90\%$ electrical test yield consistently over multiple lots of build for single layer DBI bonding. We did not see any yield loss due to bond misalignment. Instead the yield loss was usually due to a defect preventing a continuous bond at the interface. With optimization for a die stacking process, we achieved an equivalent per-layer void free yield for all 5 layers in the TSV die stack. The per-layer assembly yield data is collected by analyzing CSAM images from the 5 interfaces of the completed 5-layer stack. The per-layer yield is calculated by counting all void-free die and dividing the number by the total number of die bonded.

Table I shows the yield of all 5 layers in the stack. There is no significant difference between the layers. The compound void-free yield for the entire stack is 60%. Resistivity measurement on the main TSV chain in the center area of the die with $>47,000$ interconnects through the 5-layer stack resulted in test yield of 66%. This is expected since some parts have voids away from the center TSV area. The voids in these die will not interrupt electrical connection of the TSV daisy chain. We have shown previously that voids in the single layer part did not grow through 2000 cycles of temperature cycling from -40°C to 150°C . Void stability in the TSV stacked package will be examined once the reliability testing is complete.

TABLE I. VOID FREE BONDING YIELD PER LAYER IN A 5-LAYER STACK

Layer	Void free bonding yield
Layer 1	90%
Layer 2	87%
Layer 3	92%
Layer 5	93%
Layer 5 (CAP)	89%
Total Yield (5-layer stacks without void)	60%

Fig. 4a shows a SEM cross-section image of 5-die TSV stack module. Fig. 4b shows a cross sectional image of typical backside TSVs to the front side DBI pad joints with and without TSV. Solid Cu-Cu bonding was formed after the $200\text{-}250^\circ\text{C}/1$ hour anneal.



(a)

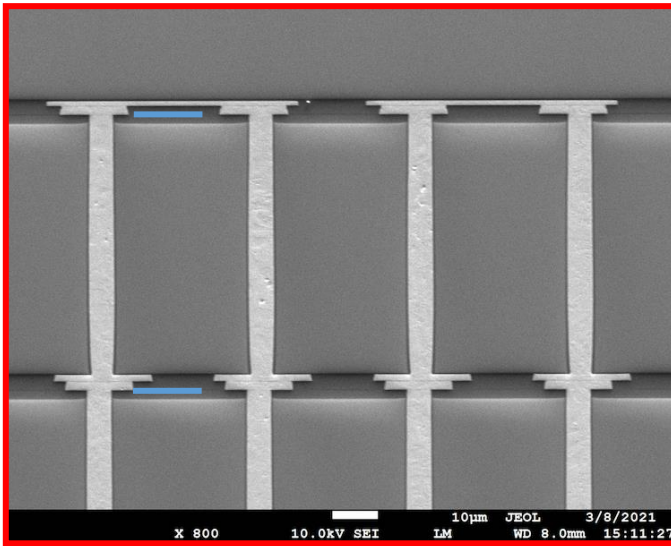


Fig. 4. a) SEM cross-section image of a 5-layer stack parts showing the TSVs integrated with DBI bonding and daisy connection. b) A representative SEM image of TSV to DBI pad joints cross-section. The blue lines mark the bonding interfaces.

D. Preparation for Reliability Test

After measuring the resistance on each 5-die stack at the wafer level, we plated a metal layer stack appropriate for reliability testing on the host wafer. The host wafer was singulated and the resistance of the individual 5-die stack modules were tested to verify no change in the test chain resistance. A time zero scan was obtained for CSAM measurement on the singulated module to ensure no change in the void analysis within the 5-die stacks. After the post-dicing characterization was complete, the parts were divided for the following reliability tests: autoclave, high temperature storage, moisture sensitivity and temperature cycling.

IV. RELIABILITY TESTING

1) Autoclave Test

The 5-die stack modules (22 parts) completed autoclave testing per JESD22-A102D spec. The test condition is 121°C/100% RH, 15 psi, for 168 hours. The JEDEC requirement is less than 10% increase in resistance after the test. All parts passed the test. As shown in Fig. 5, The average resistance increase is less than 1%. CSAM analysis after the autoclave test showed no change in voiding pattern or void size. The results are consistent with prior results on single layer samples[8]. The results confirm that the hermetical seal offered by the bonded dielectric surrounding the Cu interconnects is also effective in preventing ingress of moisture to the Cu joint and TSV within the stacked package and protected it from corrosion.

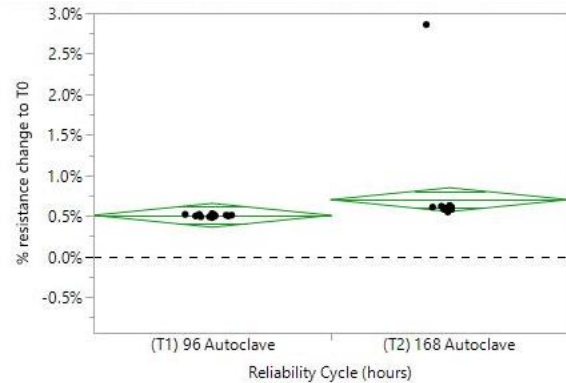
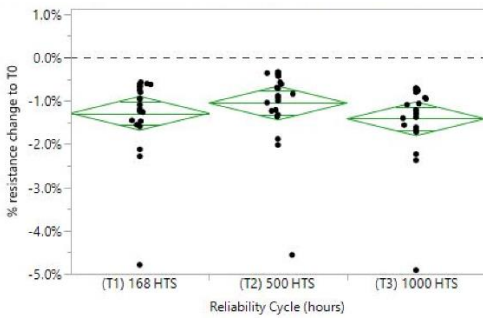


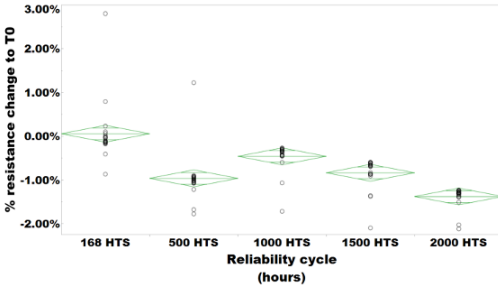
Fig. 5. Resistance change vs time zero for the modules in autoclave test at two read-out points.

2) High Temperature Storage Test

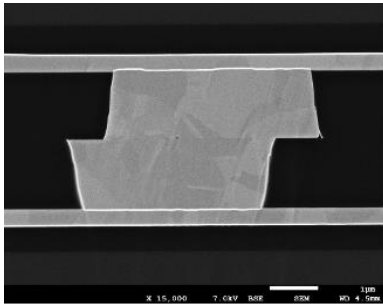
The hybrid bonded modules (22 parts) are currently in high temperature storage testing per JESD22-A103 Condition G (150°C). The requirement for DRAM packages is 1000 hours with a resistance increase less than 10%. Electrical testing data at 168, 500 and 1000 hours are shown in Fig. 6a. The resistance showed no increase after the test. Instead, a slight drop of ~1% is observed. This behavior is different from solder interconnects for which resistance increases after high temperature storage. However, the trend is consistent with prior high temperature storage test data on single layer DBI bonded parts. As shown in Fig. 6b, after 2000 hours at 225°C, the daisy chain resistance decreased by ~1.3%. Cross section analysis of a single layer part after 2000 hours at 225°C showed no sign of Cu oxidation, corrosion or void growth at the Cu-Cu bonding interface (Fig. 6c)



(a)



(b)



(c)

Fig. 6. (a) Resistance change of the 5-die TSV stack module in high temperature storage test at 150°C; (b) Resistance change of a single layer part in 225°C storage; (c) Cross-sectional SEM image of a single layer part after 2000 hours at 225°C showing absence of sign of corrosion, oxidation or void growth.

The absence of a resistance increase in the high temperature storage and void growth in the single layer parts can be explained by two fundamental advantages of the DBI bonding: hermetical seal of the Cu interconnects by the surrounding oxide and of the energetically stable monolithic Cu joints because there is no intermetallic formation [14]. The slight drop in resistance can be attributed to improved metallurgical bonding at the joint interface with additional Cu anneal during the environmental test. Based on the trend of slightly decreasing resistance after 1000 hours, these factors appear to be equally effective in preventing degradation of the TSV stacked parts when integrated with a hybrid bond in place of the typical solder interconnect. Test will continue to 2000 hours. Further CSAM measurement and cross section analysis will be conducted on the stacked TSV parts after completion of the 2000-hour test.

3) Moisture Sensitivity Test

The 5-die stack modules (22 samples) have completed moisture sensitivity test per J-STD-020D.1 MSL3 standard. The samples were first baked at 125°C for 24 hours, then soaked at 30°C/60% RH for 192 hours, followed by 3 times reflow at 260°C peak temperature. Resistance measurement and CSAM measurements were carried out before and after the tests. The modules showed no change in resistivity and no change in voiding patterns or void size.

4) Temperature Cycling Test

The 5-die stack hybrid bonded modules (45 samples) are pre-conditioned per JEDEC Standard 22-A113D moisture sensitivity level 3 (MSL3) requirements. The samples were first baked at 125°C for 24 hours, then soaked at 30°C/60%RH for 192 hours, followed by 3 times reflow at 260°C peak temperature. Following the pre-condition, the parts are subjected to temperature cycling test per JESD22-A104D specification Condition G (from -40°C to 125°C). The JEDEC requirement is 1000 cycles with a resistance increase less than 10%. First read-out point at 250 cycles showed no change in resistivity. Full results will be reported in the conference presentation in June.

We have published temperature cycling test results on single layer D2W bonded DBI parts in 2018 [8]. The parts showed no resistance increase after 2000 cycles from -40°C to 150°C and cross section analysis of the post-test parts showed no sign of Cu oxidation, corrosion or cracking. The superior performance of the parts can be attributed to three factors: 1) hermetical seal offered by the surrounding dielectric prevents Cu oxidation, 2) Elimination of underfill and solder bump means there is no CTE mismatch between the top and bottom die of the bonded joints, there is no driving force for crack initiation. 3) No intermetallic formation.

These three factors that give the single layer part superior temperature cycling performance remain exist in the 5-die stack module with TSVs, we anticipate a similar strong performance.

Table II gives a summary of completed and ongoing reliability tests for the stacked modules with TSV.

TABLE II. COMPLETED OR IN PROGRESS RELIABILITY TESTS ON 5-DIE STACK MODULE

Test	Standard	Test Condition	Sample size	Status
Autoclave	JESD22-A102D	121°C/100%RH, 15psi, 168 hours	22	Completed, all pass
High Temperature Storage	JESD22-A103	150°C, 1000 hours	22	In progress No failure after 500 hours
Moisture Sensitivity Test	J-STD-020D.1	MSL 3	22	Completed, all pass
Temperature Cycling with MSL3 Pre-conditioning	JESD22-A104D Condition G	-40°C to 125°C, 1000 cycles	45	In progress

V. DISCUSSION

Compared to D2W stacking with solder micro bumps, stacking with hybrid bonding offers multiple advantages.

A) Height Advantage

Solder bump and underfill are essential components of the stacked micro bump package. They add approximately 20 μm to each layer. By comparison, stacking with hybrid bonding totally eliminated the solder bump/underfill layer and frees up vertical space to allow packaging of more layers without exceeding the system overall height limit.

B) Cost Advantage

The process flow we have developed is similar to the flow for fabrication of a TSV die with solder micro bumps. However, with the elimination of the UBM stack and micro bumps on the front side and the solder pad on the backside, the DBI die fabrication process is more streamlined than the microbump die fabrication. A detailed comparison between the the TSV die for DBI bonding and the TSV die for solder microbump was discussed previously[12,13].

C) Density advantage

Solder micro bumps have approached their physical pitch scaling limit. Bond pitch in volume manufacturing has been stagnant around 35-40 μm for several years. By comparison, the physical limit of hybrid bonding is sub-micron. The main limiting factor for fine pitch is bonder alignment capability. Xperi has demonstrated 2 generations of bond pitch scaling with D2W bonding (10 μm pitch). In 2020 Besi reported their Chameo 8800 Ultra Plus bonder, which has 200 nm placement accuracy for hybrid bonding at 2,000 UPH [15]. This will enable fine pitch designs of ~ 2 μm for high volume production. Additionally, bonding at sub-micron pitch has been demonstrated by TSMC[16].

D) Performance Advantage

Xperi's thermal and electrical simulation studies showed that the stacked DBI package showed enhanced thermal

performance as well as electrical performance >5GHz [17]. Significant electrical performance enhancement has also been reported by TSMC[18].

E) Reliability Advantage

An all Cu, direct bond interconnect demonstrated here eliminates multiple factors that cause parts to fail in service.

1) Hermetical Seal within the Bonded Dielectric Surrounding the Cu Joints

As noted above, the distinctive advantage of the direct bond joints is the protection by the surrounding dielectric. To evaluate the effectiveness of the bonded dielectric as hermetical seal, we bonded silicon wafers with etched cavities and diced the wafer pair into parts with a single cavity. The oxide bond line width at the outer edge of the cavity varied from 8 μm to 280 μm . Singulated parts were submitted to Oneida Research Service in Colorado for leak test. The results are shown in Fig. 7. The helium leak rate does not show any dependence on the bond line thickness. A bond line as thin as 8 μm can provide helium leak rate below 10^{-11} atm-cc/s. Since a package with helium leak rate below 5×10^{-8} atm-cc/s is designated as hermetic package[19], The hermetical seal offered by the bonded oxide far exceeds such requirement. This hermetical seal is one of the main reasons for the high reliability of the single layer DBI parts we tested previously [8].

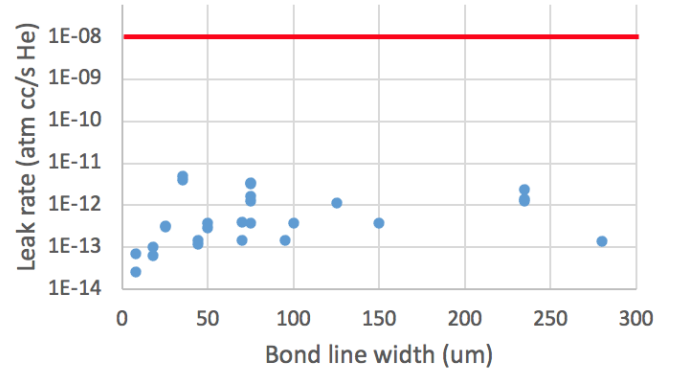


Fig. 7. He leak rate of cavity die with Zibond seal vs the bond line width. The red line marks threshold for hermetic package[19]

As shown in Fig. 7, the bonded oxide surrounding the joints offers superior hermetical protection, preventing Cu oxidation and corrosion. Therefore, the technology is ideal for automotive parts that operate in high temperature environment underhood, or are exposed to corrosive environment such as exhaust gas or very polluted air.

2) Eliminating CTE Mismatch

CTE mismatch between the silicon, solder and underfill is the fundamental driving force of crack initiation and growth during temperature cycling. Eliminating solder and underfill from the package not only reduces package cost,

package height, it also significantly enhances thermal-mechanical reliability of the part.

3) Eliminating Intermetallic Formation

Formation of intermetallic compounds in solder joints is unavoidable. Volume shrinkage during the intermetallic formation leaves behind voids. Most intermetallic compounds are also brittle and fractures easily. The monolithic Cu DBI joints totally eliminate intermetallic formation and associated problems.

In summary, the 5 die stack modules were prepared in a prototype line to show that each hybrid bonded layer gave equivalent assembly yield indicating the viability of scaling the hybrid bonding stacking process within the packaging industry. The thermal budget for the all-Cu interconnect package was 250°C for 1 hour. The advantages of hybrid bonding over a flip chip interconnect with solder micro bump and underfill were outlined and point to opportunities to reduce overall costs, to continue pitch scaling while obtaining a package with improved electrical, thermal performance and reliability with an all Cu hybrid bonded interconnect at a low thermal budget .

VI. SUMMARY

This study reinforces the unique advantages of using an all Cu, hybrid bond interconnect for improved reliability in the next generation of advanced packaging. Specifically, the assembly yield for stacking was shown to be consistent for all layers within the 5-die stack TSV-based module. Enhanced reliability performance was measured in several of the environmental tests. The dielectric hermeticity test results suggest that the dielectric surrounding the Cu joints offer a superior hermetic seal compared to standard interconnects which are surrounded by underfill. The hybrid bonded interconnect is well suited for applications in high temperature and/ or corrosive environments such as automotive exhaust.

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