

Die to Wafer Hybrid Bonding and Fine Pitch Considerations

Thomas Workman
Invensas
Xperi Corporation
San Jose, CA, USA
Thomas.Workman@Xperi.com

Laura Mirkarimi
Invensas
Xperi Corporation
San Jose, CA, USA
Laura.Mirkarimi@Xperi.com

Jeremy Theil
Invensas
Xperi Corporation
San Jose, CA, USA
Jeremy.Theil @Xperi.com

Gill Fountain
Invensas
Xperi Corporation
San Jose, CA, USA
Gill.Fountain @Xperi.com

KM Bang
Invensas
Xperi Corporation
San Jose, CA, USA
KM.Bang @Xperi.com

Bongsub Lee
Invensas
Xperi Corporation
San Jose, CA, USA
Bongsub.Lee @Xperi.com

Cyprian Uzoh
Invensas
Xperi Corporation
San Jose, CA, USA
Cyprian.Uzoh @Xperi.com

Dominik Suwito
Invensas
Xperi Corporation
San Jose, CA, USA
Dominik.Suwito @Xperi.com

Guilian Gao
Invensas
Xperi Corporation
San Jose, CA, USA
Guilian.Gao@Xperi.com

Pawel Mrozek
Invensas
Xperi Corporation
San Jose, CA, USA
Pawel.Mrozek@Xperi.com

Abstract—Hybrid bonding is becoming increasingly important as the semiconductor industry plans for the next generation of packaging where high bandwidth architectures are required to achieve improved compute performance demands. The scalability challenges in solder-based interconnects at $<35\ \mu\text{m}$ pitch has fueled the adoption of hybrid bonding as a technology with enhanced scalability. The direct bond interconnect (DBI®) technology which was developed originally for wafer to wafer (W2W) applications has been extended to die to wafer (D2W) as DBI® Ultra.

In this paper, we discuss the test results for a new die to wafer hybrid bonding test vehicle with an interconnect design of $2\ \mu\text{m}$ pad on $4\ \mu\text{m}$ pitch. The $8\ \text{mm}$ by $12\ \text{mm}$ chip contains daisy chain test structures ranging from 126,000 to 1,600,000 links. The component die wafers were singulated with conventional stealth dicing and then processed on tape frame for preparation of D2W bonding. The $2\ \mu\text{m}$ bond pad requires sub-micron alignment accuracy within the pick and place tool for 100% alignment yield. However, due to bonder availability, our initial trials were bonded on a Besi Chameo Advanced bonder with an ISO 3 bonding environment and an alignment accuracy of $\pm 3\ \mu\text{m}$ (3σ). The bond quality is characterized with C-mode scanning acoustic microscopy (CSAM), electrical resistance measurement, and cross-section microscopy analysis. The bond yield is shared as a function of bond defect density and electrical yield. Daisy chain yield and resistance versus misalignment for the fine pitch test vehicle are compared to test vehicles having a $10\ \mu\text{m}$ pad on $40\ \mu\text{m}$ pitch. The implications of the $10\times$ pitch shrink on process control from wafer and die fabrication are discussed.

Keywords— low temperature Cu to Cu direct bonding, direct bond interconnect (DBI), DBI Ultra, hybrid bonding, D2W, fine

pitch, high accuracy die bonding, clean die bonder, die deformation, HVM

I. INTRODUCTION

The semiconductor industry is adopting hybrid bonding in step with market demands for applications where the incumbent technology has run out of steam. Hybrid bonding adoption is a function of the benefit over existing chip interconnect technologies and the capability of process equipment sets to manufacture components via hybrid bonding with high yield and reasonably equivalent cost to other available methods. Direct Bond Interconnect (DBI®) is the platform technology that Xperi is developing to advance industry understanding and commercial adoption of hybrid bonding in the electronics industry. The many process benefits of hybrid bonding over other technologies, such as thermo-compression bonding of micro-pillars, include room temperature, low stress bonding; lack of bumping and underfill, etc.; and are explained in detail in [1, 2, 3, 4].

To date, wafer-to-wafer (W2W) hybrid bonding has been demonstrated at pad size and pitch as small as $1\ \mu\text{m}$ pad on $2\ \mu\text{m}$ pitch [5, 6]. However, for die-to-wafer (D2W) products, the lack of equipment capable of bonding at sub-micron accuracy with high speed and yield has delayed the ability to implement hybrid bonding for pad sizes below $5\ \mu\text{m}$.

The two major improvements needed for flip chip bonders to be capable of high-yield, high-throughput hybrid bonding at fine pitch ($< 2\ \mu\text{m}$ pad diameter) are improved alignment accuracy and improved cleanliness. As most HVM-capable flip-chip bonders have alignment tolerances of $\sim\pm 3\ \mu\text{m}$ (3σ) or higher, bonding devices with pad size below $5 - 10\ \mu\text{m}$ is not

feasible. For a bonder to be capable of high-yield bonding of fine pitch products, the alignment tolerance of the bonder will need to be better than 0.1 – 0.25 times the pad diameter, or 200 – 500 nm for 2 μm pads.

Hybrid bonding requires the environment inside the bonder to be clean enough to prevent particle contamination of the substrate wafer and component die during ejection, flipping, alignment, and bonding. Because the bonding surfaces are flat to the nanometer scale, any particle contamination can prevent the surfaces from connecting and forming a bond in the local area of the particle. Sensitivity to particle contamination scales roughly with pad size and pitch, so fine pitch products will generally need an ISO 3 environment or better, controlling particle size down to $\sim 0.2 \mu\text{m}$.

As equipment suppliers are bringing to market flip chip bonders that meet the sub-micron alignment requirement [7] few are focused on the overall hybrid bonding process needs of alignment, cleanliness, and low force [8, 9]. We have created a fine-pitch test chip to validate equipment sets and process flows for D2W fine pitch hybrid bonding.

II. FINE PITCH TEST VEHICLE

A. Design Considerations

A 2 μm pad on 4 μm pitch was chosen for this test vehicle for several reasons. First, it is within the fabrication capability of our foundry partners, with only small variations from their design rules. Second, yield results for this test vehicle can be compared to data we have already collected on W2W test vehicles with similar pad and pitch design. Third, it is expected to have high yield on a Besi Datacon 8800 CHAMEO^{ultra plus} bonder, with specified alignment tolerance of $\pm 200 \text{ nm}$ (3σ). Fourth, it is expected to have significant yield ($\sim 50\%$) on our Besi Datacon 8800 CHAMEO^{advanced} bonder, even though the pad size is smaller than the alignment tolerance of bonder. This will allow us to collect some initial results with our in-house bonder and allow direct comparison to results from our test vehicles with larger pad & pitch processed on the same equipment.

The chip size was set at 8 x 12 mm because it will be directly comparable to our other test vehicles of the same size, and it will allow the use of the same tooling. Also, it is of sufficient size to be able to examine the effects of both translational and rotational alignment errors. For the Chameo Advanced bonder, alignment results from similar sized test chips show that we can expect a variation of approximately $\pm 2 \mu\text{m}$ in x and y, and $\pm 12 \text{ m}^\circ$ in rotation. At the die corners, the offsets due to translational and rotational variation will be roughly equivalent, and roughly the same size as the pad diameter.

B. Test Structures

The test vehicle includes five daisy chain arrays that can be tested to check for electrical connectivity (Fig. 1). These arrays were sized and positioned to be similar to those used on previous test chips to facilitate comparison. Then main, central array (DC) has an area of 50 mm^2 and contains 1.6 million links. It is divided into nine horizontal sections, each individually testable. Comparison of yield between these nine equal sub-arrays can be used to determine the effect of rotational misalignment. The top

and bottom arrays (DCT & DCB) have areas of 6 mm^2 with 191,000 links each. The left array (DCL) has an area of 8 mm^2 with 253,000 links, divided into two horizontal divisions that are individually testable. The right array (DCR) has an area of 8 mm^2 with 253,000 links, divided into two intertwined serpentine chains that are individually testable (Fig. 2). This array is designed so that leakage current between the arrays can be checked for leakage across 126,000 links at 2 μm spacing.

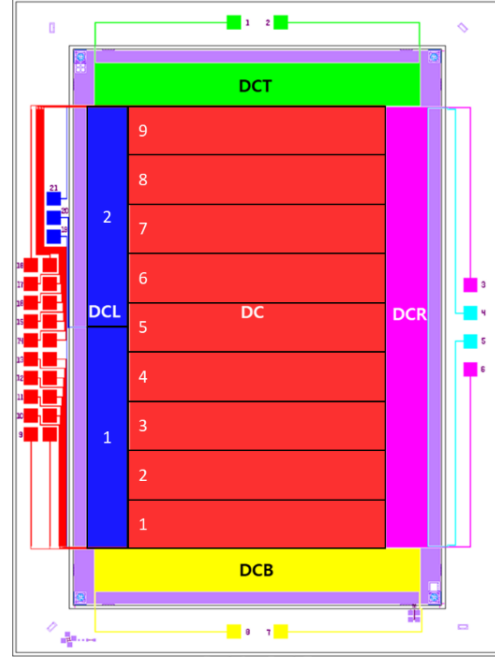


Fig. 1. Fine pitch hybrid bonding test chip layout showing the five daisy chain arrays made up of the main, center array (DC) with nine sub-chains (1-9), top and bottom arrays (DCT & DCB), left array (DCL) with two subchains (1-2), and right side array (DCR) with two intertwined serpentine sub-chains.

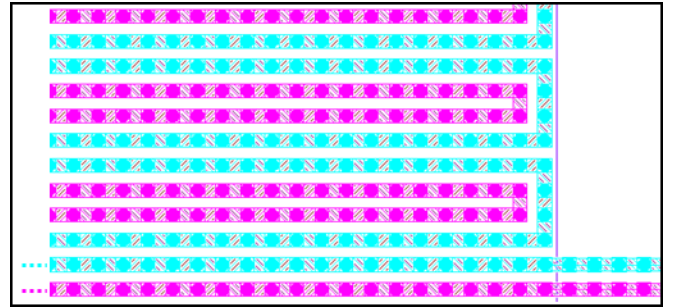


Fig. 2. Detail of right daisy chain array showing the intertwined serpentine chains Right 1 (pink chain) and Right 2 (blue chain). These chains are used to check for any leakage between adjacent links.

C. Alignment Features

Alignment features are included on all corners of the component die and substrate bonding sites (Fig. 3). The main features for alignment by the bonder are concentric annuli on the die corners of the component die and substrate, following Besi's recommendations for high accuracy alignment [8]. Each corner also contains vernier structures for manual post-bond alignment measurement. The verniers have resolution of 0.25 μm for the corner structure and 0.1 μm for the horizontal and vertical verniers adjacent to each corner. Higher precision alignment

measurements can be made using pattern recognition on the concentric annuli.

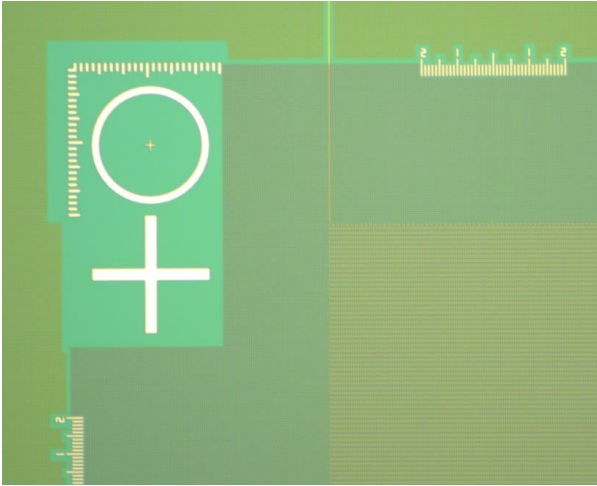


Fig. 3. Microscope image of substrate die corner showing circle and cross alignment fiducials and verniers for measuring bond alignment.

D. Layer Structure and Fabrication

The 200 mm substrate and component die wafers were fabricated at Tower Semiconductor, using their standard single damascene Cu metallization process. The redistribution layer (RDL) is 0.9 μm thick Cu damascene metallization in silicon dioxide. The top layer contains the 2 μm diameter DBI bond pads, formed using a 3.3 μm thick Cu damascene process. Thick metal layers were chosen to minimize the resistance of the daisy chain so that any increased resistance from poor alignment or metal-to-metal bonding would be easier to detect. Wafer processing was performed at Tower Semiconductor up to the DBI layer Cu plating. All subsequent processing was performed by Xperi.

III. PROCESS FLOW

Once received by Xperi from the foundry with blanket top layer metallization, the copper and dielectric of the substrate wafers were thinned by CMP until the specified dielectric flatness and metal recess were achieved. This was followed by a thorough cleaning step to remove any debris or surface contamination from the CMP process, and then a plasma activation to prepare the dielectric for a high-strength chemical bond.

The component die wafers underwent a similar CMP process to create the same flat surface. The wafers were mounted on tape on a dicing frame for thinning, dicing, post-dicing clean to remove any dicing debris, and then plasma activation. Both mechanical saw dicing and stealth dicing have been used for singulation.

Die were then bonded to substrate wafers in a flip chip bonder at room temperature with minimal bond force. The activated dielectric surfaces bond spontaneously upon contact. After all die were bonded, the substrates were annealed in a batch oven at temperatures ranging from 300 - 400°C, which causes the metal bond pads to contact and interdiffuse to form a metallurgical bond.

Final wafer cleaning, activation, bonding, and anneal were performed in Xperi's prototyping laboratory in a Class 1000 cleanroom. Manual handling of wafer and dicing frames was required to load and unload material at each process step and to transport material between steps, which results in a minor amount of added particle contamination. Bonding was performed on a Besi Datacon 8800 CHAMEO^{advanced} bonder with an ISO 3 clean kit to keep the bonding environment as clean as possible. Surfscan monitors performed within the bonder on wafers in the substrate and component positions show an average of ~ 1 particle $>0.3 \mu\text{m}$ per pass of 260 simulated bonds. Additional bonding using a Besi Datacon 8800 CHAMEO^{ultra plus} bonder with a similar ISO 3 clean kit and bonding accuracy of 200 nm (3σ) is expected to be performed but was not completed at the time of paper submission.

After anneal, IR imaging of each bonded die was performed to determine alignment offset (x, y, θ) by reading the verniers in opposite die corners (Fig. 4). C-mode scanning acoustical microscopy (CSAM) was performed to detect any bond interface voids, and electrical testing was performed to measure the resistance of the daisy chain arrays on each die. Alignment, voiding, and electrical data were combined to analyze the effect of alignment and voiding on electrical resistance of the test structures. Finally, cross-sectional SEM was performed to assess the post-anneal metal and dielectric bond quality.

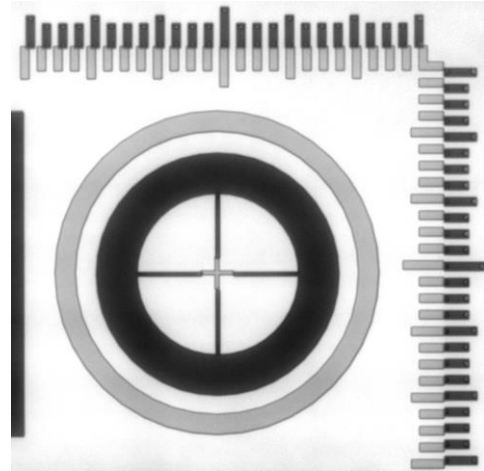


Fig. 4. Post-Bond IR image of die corner showing annuli fiducials (used by bonder for alignment) and verniers (for manual alignment measurement)

IV. RESULTS

A. Alignment

A total of three lots were bonded. Alignment was consistent between lots, with die center offset of $0.94 \pm 0.46 \mu\text{m}$, and die rotation of $-0.1 \pm 3.7 \text{ m}^\circ$ (Fig. 5). This is a slight improvement on alignment for similar sized coarse pitch test vehicles and is attributed to the improved high contrast circular alignment marks. Due to die rotational misalignment, each daisy chain array will have a slightly different bonding offset depending on its position on the die.

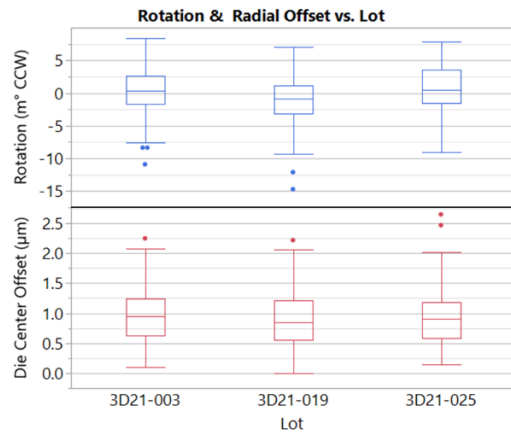


Fig. 5. Alignment accuracy for the three bonded lots. Distribution of die rotational angle and the radial die center offset were consistent between the three lots.

Using the (x, y, θ) misalignment for each die, the local misalignment (local offset) was calculated for each daisy chain array so that electrical resistance and yield could be compared to the misalignment within the chain. The variation in pad offset by array for a typical lot is shown in Fig. 6. As expected, arrays farther from the center of the die have larger offsets than those near the center due to die rotation. Less than 10% of arrays had misalignment of more than $2\ \mu\text{m}$ (the bond pad diameter), and more than 80% of arrays had misalignment of less than $1.5\ \mu\text{m}$ and would be expected to make good electrical connections.

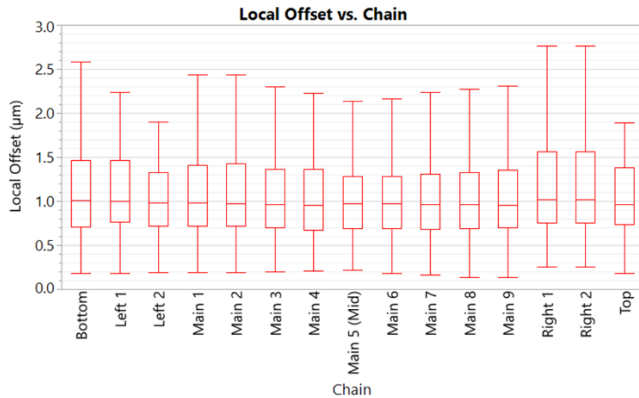


Fig. 6. Local offset distribution for each of the sub-chains on the die across one bonded lot, showing slightly worse alignment for the bottom and right daisy chain arrays compared to the center.

B. Voiding

Voiding as detected by CSAM occurred in 3-5% of the bonded die in the three lots. Void shape, size, and position were consistent with voids caused by particle contamination during manual handling. The low level of voiding on these fine pitch lots was similar to that observed in other test chips of similar size. The voids only caused electrical failures (open circuit) in arrays that were intersected by the void; adjacent arrays were unaffected. The CSAM image from Lot 1 (Fig. 7) is typical. Empty sites in the interior of the bonded region are defective substrate sites which were intentionally skipped during bonding.

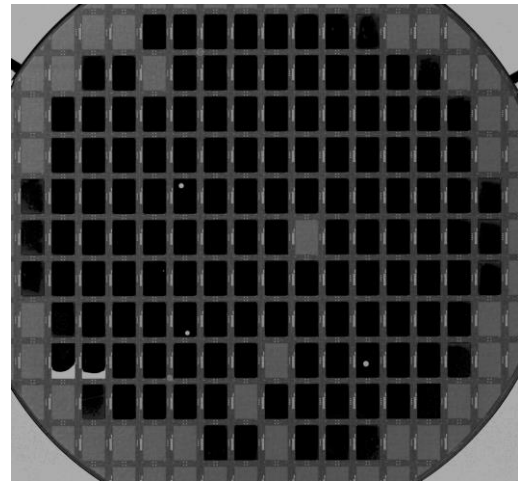


Fig. 7. CSAM image of bonded wafer, showing edge or circular voids on 4% of bonded die.

C. Hybrid Bond Quality

Cross-sectional SEM images were taken of bonded die after anneal. Fig. 8 shows a segment of the center daisy chain array. The dielectric-to-dielectric bond is free of gaps, and the Cu bond pads have fully connected. This shows successful CMP surface planarization, die surface cleaning, activation, and sufficient anneal time and temperature to create a robust electrical connection. Based on these images, it was determined that a post-bond anneal of 300°C was sufficient to fully connect the Cu DBI pads.

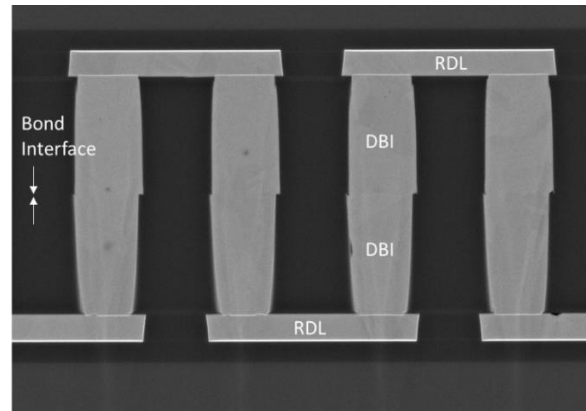


Fig. 8. Cross-sectional SEM image of main daisy chain array after anneal showing good alignment and high quality of dielectric-dielectric and metal-metal bonding.

D. Electrical Yield

The resistance of the daisy chain array is the sum of the resistance of the RDL traces, DBI bond pads, and the contact resistance at the bond interface of each link. The contact resistance will be at a minimum for perfectly aligned bond pads that are fully connected without gaps. Any increase in resistance from the minimum will then be due to the combination of misalignment and defects at the bond interfaces of each of the links in the array or due to defects inherent in the wafers (such as missing metal, poor connectivity between RDL and DBI layers, etc.). As there is no redundancy in the chains, a single

fully misaligned or fully voided interconnect will result in an open circuit failure of the chain.

The theoretical resistance of the daisy chains on this test vehicle is 23 – 35 k Ω (depending on the number of links), and failed arrays are expected to have resistance >1 G Ω . We define an array as connected if its measured resistance is less than ten times its theoretical resistance. If the resistance is within 50% of its theoretical resistance, it is counted as passing. Each of the sub-chains of the five arrays was measured individually, for a total of 15 sub-chains per die.

Connected and passing yield for the three lots tested is shown in Fig. 9. The passing yield varied from 30 – 53%, with the sub-chains closer to the center of the die generally yielding better than those near the die edges. The connected yield was 6 – 10% higher than the passing yield, indicating a significant fraction of the die had marginal connectivity at some point within the chain.

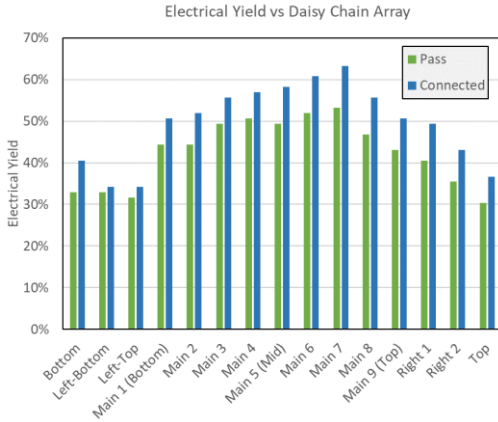


Fig. 9. Electrical yield for each of the sub-chains of the five arrays on the test chip. Connected yield includes chains with resistance less than ten times the theoretical resistance. Passing yield includes chains with resistance within $\pm 50\%$ of the theoretical resistance.

V. ANALYSIS

Since new test vehicles generally achieve >90% yield [5, 10, 11], the low passing yield for the initial bonding tests of this fine pitch test vehicle indicate a problem that must be addressed. Previous experience on a variety of test vehicle pad sizes and pitches lead us to believe that the issue with this material is likely due to a fabrication defect in the test vehicle. To further explain we compare to results from a similar hybrid bonding test vehicle with 10 μm pads on 40 μm pitch (coarse pitch) that performs as expected. With that test vehicle we performed an alignment skew to cover a misalignment range of 15 μm , which is 1.5 times the pad diameter, equivalent to the misalignment range on the fine pitch material.

A. Yield vs. Misalignment and Voiding

Concentrating on the sub-chains of the fine pitch test vehicle main array, the distribution of passing chains versus local offset (Fig. 10a) shows that all passing chains have a misalignment of less than 1.6 μm (80% of the pad diameter) and passing yield for offsets less than that are in the range of 40 – 60%. The comparable plot for the coarse pitch test vehicle (Fig. 10b) shows a similar trend of passing chains being limited to offsets

of less than 80% of the 10 μm pad diameter. However, the passing yield for misalignments of less than this critical 80% offset is ~93%.

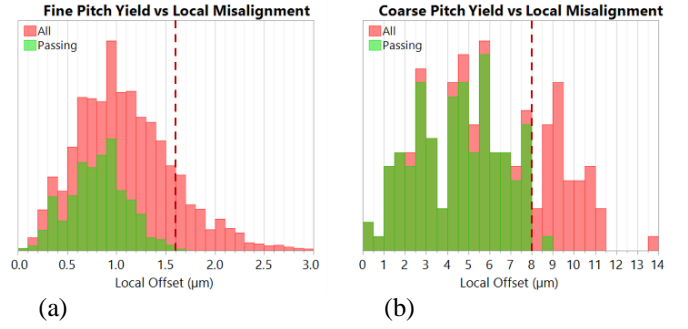
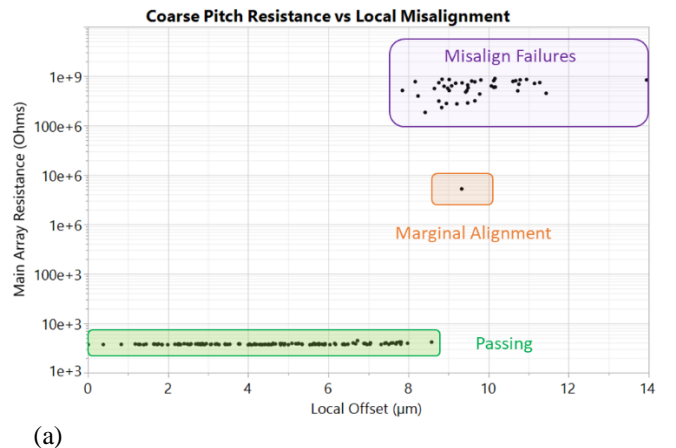


Fig. 10. (a) Fine pitch test vehicle distribution of all chains and of passing chains of the main array versus bond misalignment within the chain. All passing die had misalignment of < 1.7 μm for 2 μm bond pads. (b) Coarse pitch test vehicle distribution showing passing chains out to 8 μm for 10 μm bond pads.

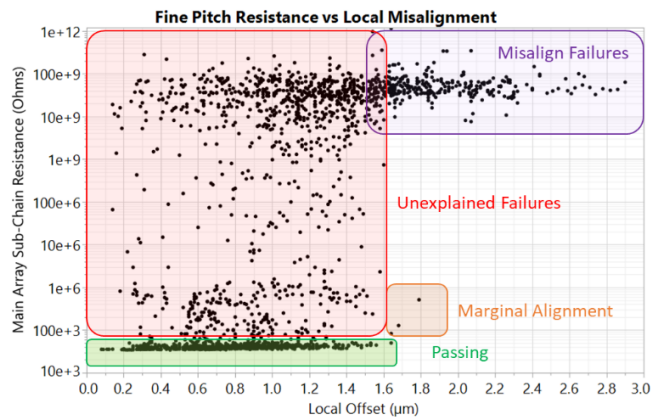
The 7% of chains in the coarse pitch test vehicle with good alignment that failed electrical test were compared against the CSAM image and were found to contain voids at the bond interface responsible for the failure. Thus, all yield loss for the coarse pitch test vehicle could be traced to either misalignment (>8 μm) or voids in the array. A similar correlation to voiding on the fine pitch test vehicle accounted for only 2% yield loss, since most of the voids were small enough that they only caused a fail on a few of the nine main array sub-chains on the affected die.

B. Resistance vs. Misalignment and Voiding

A useful test to analyze results for root cause analysis is to plot the daisy chain resistance as a function of misalignment. Known fails from voids (7% for the coarse pitch and 2% for the fine pitch structures) were removed to simplify the analysis. Resistance of all main array sub-chains (passing and failing) is plotted against local misalignment for coarse pitch in Fig. 11a. Failing chain resistance values for coarse pitch are explained by misaligned chains, and one die at a transitional alignment between passing and gross failure. For the coarse pitch graph, we see the expected collection of passing chains (low resistance) in the lower left portion of the graph, and a step function at approximately 80% of pad diameter misalignment to the failed chains (high resistance).



(a)



(b)

Fig. 11. (a) Coarse pitch chain resistance vs misalignment showing passing, marginal alignment, and misaligned chains similar to those in fine pitch. Note that any void failures were removed from the graphs for clarity. (b) Fine pitch chain resistance vs misalignment, showing passing, marginal alignment, misaligned, and unexplained failures.

In contrast, the fine pitch graph (Fig. 11b) does not have a step function between passing and gross failures. Instead, a large number of failures exist within the 0 – 80% misalignment region. Specifically, for fine pitch the approximate accounting of the chain resistance values is that 42% are passing, 20% are gross failures due to misalignment, and the remaining 38% are unexplained failures that have good alignment and no voids. This last group has a wide range of resistance values from roughly double the theoretical value to gross failure. This is a clear sign that a pervasive defect in the test structure is causing the excess fails.

Careful microscopic inspection of the component and substrate wafers in visible and IR light were performed in a search for discontinuities or necking in the RDL traces that could result in a defect mode with open circuits or high resistance in the traces, but none were discovered.

Comparing this failure group to failures from historic test chips, the signature most resembles that of a discontinuity between the DBI pad and the RDL layer. On some test vehicles, this connection is made through an intervening via layer. When this has occurred, it is often attributed to an improper etch of the dielectric at the DBI pad or via layer. This type of defect would not be visible by microscope inspection but would only be detectable by cross-section, and could have very low defect density (e.g., perhaps only a few interconnects in a daisy chain of more than 100,000 links).

The standard SEM cross sections for checking the bond interface quality (such as Fig. 8) did not show any issues with the RDL-DBI interface, but an SEM image taken as part of the initial design qualification (Fig. 12) does show what appears to be residual nitride partially blocking the interface. If this type of defect occurs at a moderate density across a wafer and includes some openings that are completely blocked, it would account for the broad range of higher than expected resistance on failed chains.

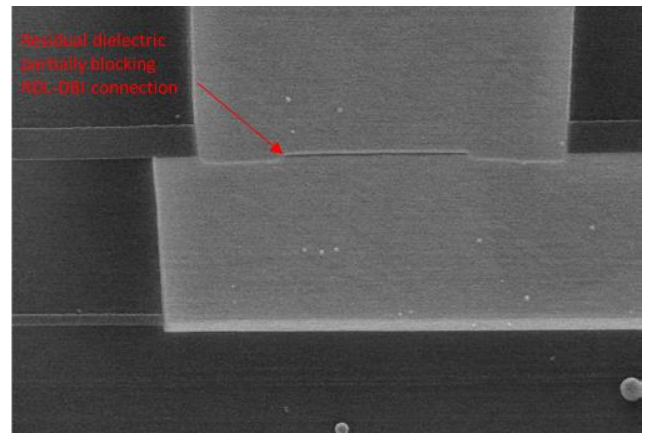


Fig. 12. SEM cross section image showing partial blockage of an RDL-DBI interface (image courtesy of Tower Semiconductor)

For the remainder of the analysis, it will be assumed that there is a random amount of excess resistance in most daisy chains, but some fraction of chains will be minimally affected by this defect and have nominal resistance.

C. Effect of Misalignment on Chain Resistance

Assuming a fixed nominal resistance of the metallization in each of the five daisy chains on the test vehicle, any increase from this baseline value in a bonded chain could be attributed to added resistance from the hybrid bond interfaces of each link. The contact area at the interface decreases roughly linearly with an increase in the radial misalignment, so the interface resistance would be expected to increase roughly linearly with misalignment until there is insufficient overlap for the Cu to make a connection, and then resistance will increase to a full open circuit value.

Resistance values of the nine identically sized main array sub-chains (DC1 – DC9) that passed electrical test were compared to the local bonding offset within each sub-chain for the fine pitch test die (Fig. 13a). As expected, there is a broad scatter in the resistance probably due to the suspected defect at the RDL-DBI interface. But even with this noise, there is a detectable increase in resistance as bond offset increases. The increase at 1.6 μm offset where there is a cut-off in connectivity is roughly 16% of the zero-offset resistance for the entire population (blue line), or approximately 35 m Ω per link. However, if only the population with minimum resistance per offset is considered (red line), the slope of the increase is considerably less, increasing by only 9% at 1.6 μm , or 20 m Ω per link.

For the coarse pitch test vehicle, the corresponding increase in chain resistance at the cutoff in continuity at 8 μm offset is slightly less at ~6%, or ~7 m Ω per link (Fig. 13b). An additional point of comparison is a W2W hybrid bonding test vehicle with an array of 115,000 links of 1.9 μm pad on 3.8 μm pitch. This showed a chain resistance increase at its cutoff offset of ~1.6 μm of 28% over the perfectly aligned value or ~50 m Ω per link [5], which is significantly higher than that for the current test vehicle.

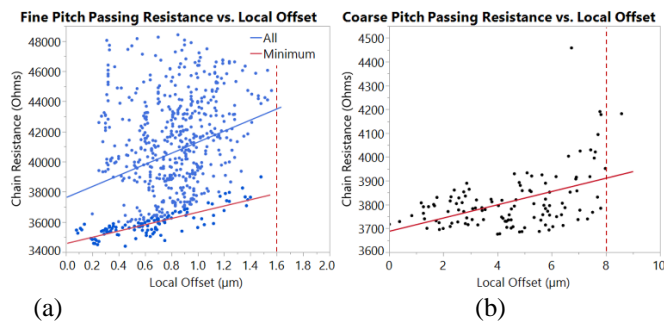


Fig. 13. (a) Fine pitch test vehicle correlation of chain resistance of passing chains to the bond offset within the chain showing trend of increasing resistance with offset. Blue line is a linear fit to all chains; red line is a linear fit of the minimum resistance. (b) Coarse pitch test vehicle correlation of chain resistance, showing a tighter distribution but similar slope to the “minimum” population of the fine pitch die.

VI. CONCLUSION

The results from the initial bonding test of the new fine pitch hybrid bonding test vehicle is an initial proof of concept of the capability of process and equipment to successfully perform D2W bonding of material with 2 μm pad size. Although the bonder used did not have the necessary alignment accuracy to achieve a high yield and the test wafers had process marginality causing random added chain resistance, useful information was still extracted from the experiment. The results indicate that daisy chain connectivity has a cut-off at 1.6 μm , or 80% of the pad diameter, which agrees with the 80% value for a coarse pitch D2W test vehicle with 10 on 40 μm pitch and a fine pitch W2W test vehicle with 1.9 on 3.8 μm pitch.

The increase in chain resistance with misalignment determined in this work is also within the range observed with the other test vehicles.

In addition, the D2W hybrid bonding process flow including CMP, substrate and die cleaning, activation, bonding, and post-bond anneal proved successful in creating a contamination-free, robust bonded interface as determined by CSAM, cross-sectional SEM, and electrical yield.

Future work will include a fix of the wafer fabrication issue and bonding in a bonder with an ISO 3 bonding environment and sub-micron accuracy that can lead to yields in the expected >90% range, which would be comparable to yields currently achieved on all of Xperi's other test vehicles.

ACKNOWLEDGMENT

Xperi thanks Besi for collaborations in bonder optimization for hybrid bonding.

REFERENCES

- [1] P. Enquist, “High density direct bond interconnect (DBI) technology for three-dimensional integrated circuit applications”, MRS Proceedings, 970, 0970-Y01-04. doi:10.1557/PROC-0970-Y01-04, 2006.
- [2] P. Enquist, “Advanced direct bond technology” in 3D Integration for VLSI Systems, S. Koester, C. S. Tan and K. N. Chen Eds, CRC Press, 2012, pp175-214.
- [3] G. Gao, et al, “Low temperature Cu interconnect with chip to wafer hybrid bonding”, IEEE 69th Electronic Components and Technology Conference, p628, 2019.

- [4] L. Mirkarimi and G. Gao, “Die to wafer hybrid bonding for 2.5D and 3D Integration”, Chip Scale Review March • April • 2020 p. 29.
- [5] Jeremy A. Theil et al., “Recent Developments in Fine Pitch Wafer-to-Wafer Hybrid Bonding with Copper Interconnect. International Wafer Level Packaging Conference, IWLPC 2019, p. 1-6.
- [6] A. Jouve, V. Balan, N. Bresson, C. Euvrard-Colnat et al., “1 μm pitch direct hybrid bonding with < 300nm wafer to wafer overlay accuracy”, Proceedings of S3S Conference, San Francisco Oct. 2017.
- [7] Nicolas Raynaud, “Considerations on the design of high precision flip chip bonder for mass production”, 3D Systems and Summit, Jan 2016.
- [8] Brandstätter et. al, “High-speed ultra-accurate direct C2W bonding”, IEEE 70th Electronic Components and Technology Conference, 2020, p1943.
- [9] Ruud Boomsma, Advanced Bonding Technologies for Next Generation 3D and SIP Devices, 3D Systems and Summit, Jan 2020.
- [10] Workman, et. al, “Cu interconnect scaling with hybrid bonding for 2.5 and 3D integration”, IMAPS Device Packaging Conference, Scottsdale, AZ, March 2020.
- [11] Gao, et. al, “Die to wafer stacking with low temperature hybrid bonding” IEEE 70th Electronic Components and Technology Conference, 2020.