Die to Wafer Hybrid Bonding for Chiplet and Heterogeneous Integration: Die Size Effects Evaluation-Small Die Applications

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***Abstract*— The Direct Bond Interconnect (DBI®) Ultra technology, a die-to-wafer (D2W) and die-to-die (D2D) hybrid bonding, is a platform technology that offers a hermetically sealed solid Cu-Cu interconnect through room temperature bonding and low temperature anneal. DBI wafer to wafer (W2W) bonding has been in high volume production since 2015. Advancement in D2W hybrid bonding technology in recent years has enabled recent adoption the technology by Sony [1]. AMD [2] and Intel [3]. The DBI Ultra D2W technology offers die-on-tape processing with bonding speeds comparable to mass reflow flip chip assembly. The bonding takes place at room temperature in an ambient environment in a class 1000 cleanroom. A low temperature batch anneal following bonding creates a solid Cu-Cu connection with no solder and no underfill.**

The value of the DBI Ultra technology can be realized in diverse products ranging from very small die to reticle-size large die. Applications such as RF, sensors and microcontrollers are in the small die domain, while GPUs and FPGAs require bonding of very large die. Ultimate SoC disaggregation implementations may include D2W bonding of mid-large sized memory die (e.g. SRAM in V-Cache) as well as ultra-small die for analog functionalities. In this paper, we present the results of D2W bonding development in die size ranging from 0.4x0.4mm to 3.2x3.0mm. The module build process includes dicing, die preparation on tape, and direct pick & place from a tape frame. The bonding quality is characterized with C-mode scanning acoustic microscopy (CSAM) and cross-section microscopy analysis.

Keywords— Cu-Cu hybrid bonding, direct bond interconnect (DBI), DBI Ultra, hybrid bonding, D2W, D2D, small die, dicing, die-on-tape processing

I. INTRODUCTION

Direct Bond Interconnect (DBI®), a low temperature hybrid bonding technology first demonstrated by Ziptronix [4, 5,6], offers numerous advantages over solder interconnect including ultra fine pitch, low package profile, protection against extreme environments (e,g, high temperature, or corrosive environment) and improved electrical and thermal mechanical performance. While applications in memory and high performance computing are driven by the demand of ultra fine pitch and electrical performance enhancement, many small form factor, low pin count applications are driven by thermal and electrical performance enhancement, thinner profile, form factor shrink; they can reap other benefits such as low profile, and high reliability demand, better real estate utility and cost savings via process node separation.

Figure 1 is an illustration of different applications that hybrid bonding can enable at different die sizes. For very small die (e.g., <0.1 mm^2) or die with similar footprint and high-test yield, W2W bonding will be more practical. However, for die size of 0.1 mm^2 and larger, D2W bonding offers more flexibility, including mismatch of die footprint and bonding multiple small dies to a base die.

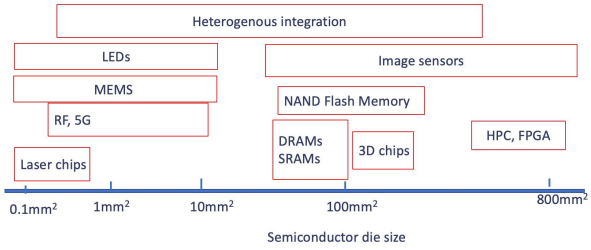

Fig. 1. Illustration of different applications that hybrid bonding can be applied at different die sizes.

Although the hybrid bonding platform technology is suitable for all die sizes, some unique challenges exist with different die size ranges. In order to maximize adpotion of the technology in diverse sectors of the semicondutor market, Xperi has conducted bonding studies with die sizes ranging from 0.4 mm to over 30 mm in linear dimensions. Figure 2 illustrates the entire range of die sizes Xperi has studied. Much of Xperi's early publications on high volume manufacturing (HVM) D2W technology targeted medium die size applications. The test die of 8 mm x 12 mm is similar to DRAM memory and chiplet applications [7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. In this paper, we present the results of our study on small die (sub mm^2 to 10 mm^2 range). Our work on bonding and characterization of very large, reticle size die will be published in a separate paper since very small die and very large die have their own unique challenges.

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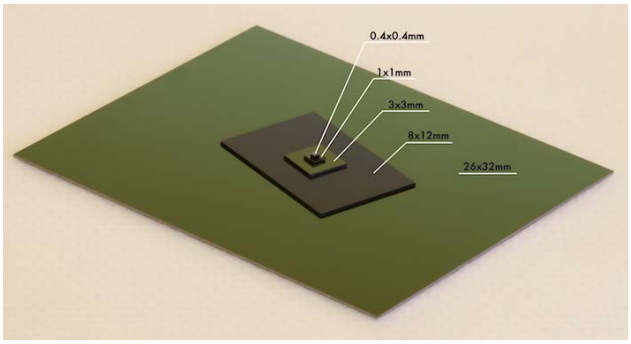
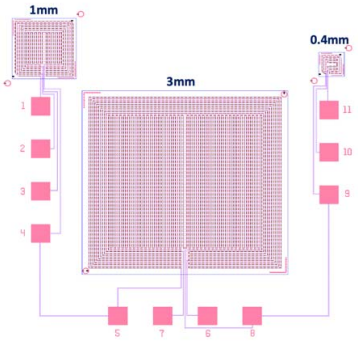


Fig. 2. Illustration of die size ranges studied by Xperi. 9 (TO BE REPLACED)

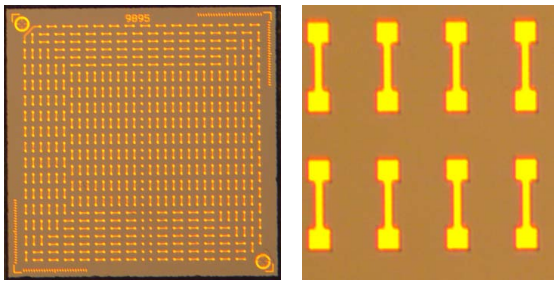
II. Test Vehicle Design and Fabrication

The phase 1 study used polished blank Si wafers with thermal oxide on the surface as the host wafer and die wafer for D2W process development. Three die sizes were chosen to represent the die size range from 0.16mm^2 to 9mm^2 area. Blank Si wafers were thinned to 200um and diced with different methods to produce dies for bonding. A surface coating was used to protect the bonding surface during grinding and dicing. The diced wafers were evaluated for die edge quality and run through the die-on-tape process for die preparation, direct ejection from the dicing tape and D2W bonding.

The phase 2 study used daisy chain wafers and die fabricated with a single Cu damascene process. Figure 3a shows a design of multi-size daisy chain substrate. It accommodates three difference die sizes: 3x3 mm, 1x1mm and 0.4x0.4 mm. Figure 3b shows a picture of a 1x1 mm die; Figure 3c shows an optical image of the daisy chain links at higher magnification. The bonding pads are 10x10 µm squares on 30 µm pitch. The 3x3 mm die has 3 chains. The total number of links for the 3 chains combined is 9488. The 1x1 mm die has three chains with a total of 926 links. Our pick and place equipment is rated to handle 0.3 mm die; however, we chose the 0.4x0.4mm so that we would not test the limit of our equipment set on the first round of experiments. The 0.4x0.4 mm die has 2 chains and 107 total links. Xperi designed and fabricated both the substrate wafers and die wafers. The CMP process has been optimized to produces very uniform and shallow Cu recess across each feature.



(a)



(b) (c)

Fig. 3. (a) Multi-size daisy chain test substrate design; (b) Image of 1x1 mm daisy chain die sigulated with mechanical saw; (c) High magnification image of individual daisy chain links fabricated with a Cu damascene process.

III. Dicing Process Evaluation

Mechanical saw is the most widely used dicing method in the semiconductor industry. However, laser stealth dicing has gained popularity with singulation of thin, large die, such as NAND memory die and DRAM die. Plasma dicing is relatively new, and currently the main application is for small die < 3 mm. Compared to blade dicing, it has superior edge quality and higher die strength. Since plasma dicing is a parallel process, it is most cost effective with small die. Compared to mechanical saw, it also has the advantage of creating an extremely narrow dicing street, allowing more area to be used to produce more die from a wafer [17]. For example, while kerf loss of ~20-50 µm is common for mechanical saw, Plasma dicing can reduce kerf loss to 4 µm. Xperi has qualified all three dicing methods for hybrid D2W bonding of 8x12 mm die. In the current study, we re-examined all three dicing methods for small die applications. Table I shows the experimental matrix for dicing evaluation using blank Si oxide wafers. There is less service capacity available for plasma dicing, so we limited the evaluation to the smallest die only. All wafers were ground to 200 µm thickness prior to dicing

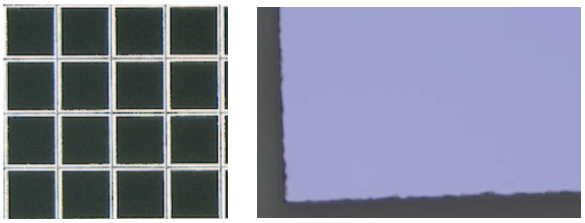
TABLE I. Dicing Evaluation Matrix

Die Size	Mechanical saw	Laser stealth	Plasma
3x3 mm		x	
1x1 mm	x	x	
0.4x0.4 mm	x	x	x

The dicing process affects edge quality on the top surface as well as damage to the diced edge and die strength. In this study, we concentrated our evaluation to the parameters that affect D2W hybrid bonding: chipping of the front bonding surface and sharp corner profile, which is critical for die picking and bonding alignment. Less emphasis was given to die strength and edge damage since the small form factors of the die and thickness to x-y size ratio make them less prone to mechanical cracking.

Mechanical saw dicing was performed by Syagrus Systems Technology in Arden Hills, Minnesota. The die edge chipping for the small die (1x1 mm and 0.4x0.4 mm) is similar

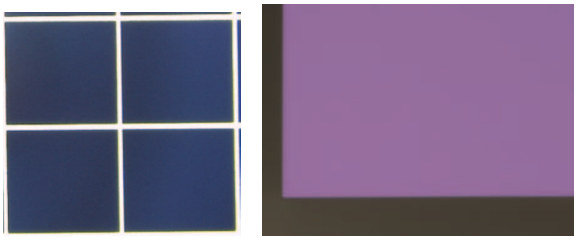
to what we observed on the larger die (8x12 mm) that was qualified for hybrid bonding. Figure 4a shows the mechanically diced 0.4x0.4 mm die on a tape frame. Figure 4b is a higher magnification image of the die corner.



(a) (b)

Fig. 4. (a) Optical image of 04x0.4 mm die sigulated by mechanical saw; (b) Higher magnification image showing quality of the die edge.

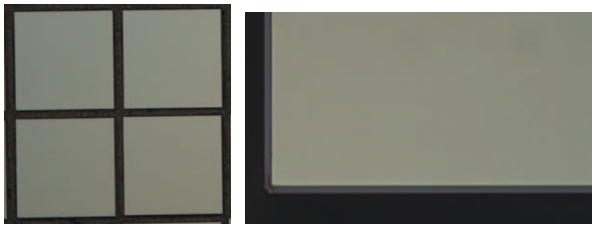
Laser stealth dicing was performed by Disco Hi-Tech in San Jose, CA. In step one, multiple passes of laser damage were injectecd into the silicon wafer at different depths. In step two, the wafer was mounted to a dicing tape frame and expanded. The lateral expansion of the dicing tape pulls the die apart to complete the singulation process [18]. The process has a limit to the die size that it can separate with clean edge for hybrid bonding. The 3x3 mm and 1x1 mm die separated successfully with straight die corners. The die edge quality is shown in Figure 5. It appears to be smoother than the saw diced die edge. The 0.4x0.4 mm die failed to separate properly using the regular tape expansion. Clearly, the amount of tape expansion was not sufficient to pull these small die apart. The unseparated 0.4x0.4 mm die were separated successfully using the Disco die separator [19] . However, the edge quality was not good enough to meet the hybrid bonding specification. Further investigation is required to assess if the process can be optimized for 0.4x0.4 mm die.



(a) (b)

Fig. 5. (a) Optical image of 3x3mm dies sigulated by laser stealth dicing; (b) Higher magnification image showing high quality of the die edge.

Plasma dicing was performed by Plasma-Therm Inc in Saint Petersburg, Florida. The wafers were first thinned to 200 µm, then patterned with 40 µm wide street opening and sent to Plasma-Therm for etching. Figure 6 shows the plasma singulated 0.4x0.4 mm die. Die edge is very smooth.



(a) (b)

Fig. 6. (a) Optical image of 0.4x0.4 mm die singulated by plasma dicing; (b) High magnification image showing high quality of the die edge.

IV. DIE-ON-TAPE PREPARATION FOR BONDING

A wafer needs to be mounted to a dicing frame for the singulation process. The DBI Ultra technology developed by Xperi use a die-on-tape process for cleaning and activation of the die for hybrid bonding. With this process, after wafer singulation, the die go through a pre-bond surface preparation while still mounted on the dicing tape in frame. This approach reduces assembly cost and minimizes die handling which can lead to die breakage and defect generation. We have shown bonding yield consistently above 95% with the 8x12 mm die using this process.

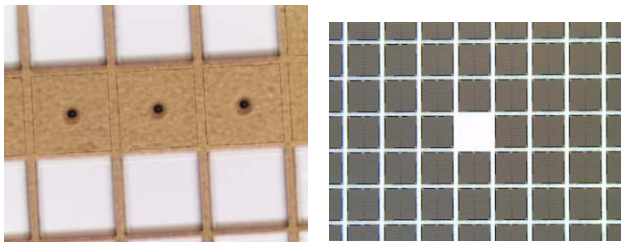
The small die in the current study have much smaller surface area in contact with the dicing frame. Therefore, die can potentially detach from the dicing tape and cause yield loss during the cleaning process. In addition, the distance of dicing street to the die center is much smaller for the small die. This could affect the fluid flow during the wet die cleaning process and impact final die cleanliness. Die detachment from the dicing tape did occur in our initial trial, The problem was solved by optimizing the overall process including the cleaning conditions. The final die surface cleanliness was equivalent for all die sizes and dicing techniques.

V. DIE EJECTION FROM A TAPE FRAME

In our HVM compatible process, the die are prepared for bonding on a tape frame which is placed inside the HVM bonder for direct die pick and place onto the host wafer. The die can be picked according to a known-good-die wafer map. A Datacon 8800 Chameo Advanced bonder with a ISO3 clean kit is used for the die picking and bonding step. The machine meets the alignment specification of 3σ (local) < 3 µm and 3σ (global) < 5 µm.

The die picking process includes physically pushing the die from the back with ejection pins to lift it partially off the dicing tape. During ejection the flip tool contacts the die bonding surface and removes the die from the tape with a vacuum force. Following the ejection process, the tool flips the die and transfers the die to the bonding tool. The bonding tool picks up the die on the backside and holds it with a vacuum force which is released when placing it on the host wafer.

It took several iterations of trial and error to optimize the die ejection process. The issues were related to the choice of the ejector pin sizes and configuration, alignment of the die and flip tool to the ejector, and ejection pin travel distance. For example, the 0.4x0.4 mm die, before the ejection process was optimized, only die with a missing neighbor could be ejected (Figure 7a). After the process optimization, a die with all four neighbors present was ejected successfully (Figure 7b).



(a) (b)

Fig. 7. (a) Optical image of 0.4x0.4 mm oxide die remaining on the tape after an ejection trial. Only die with a missing neighber were ejected successfully; (b) Empty site of a 0.4x0.4 mm daisy chain die with all four neighbors. The die was ejected successfully after process optimization.

VI. D2W BONDING EVALUATION

The dielectric-to-dielectric bonding is a spontaneous process that takes place when the cleaned and activated die surface touches the cleaned and activated host wafer surface. Bonding takes place at room temperature in an ambient environment. Since the bond is atomic scale, a clean environment is required to minimize particle contamination induced bonding voids. Xperi's prototype laboratory for hybrid bonding is a class 1000 cleanroom. A low temperature batch anneal after bonding results in solid Cu-Cu connection with no solder and no underfill.

To minimize engineering time, a program designed for bonding the 8x12 mm die to a host wafer was re-used for the initial bonding evaluation of 0.4x0.4 mm and 1x1 mm die. Nine dies were bonded closely as a cluster to each programed sites on the host wafer. All dies picked from the tape frame were bonded successfully with no bond fails.

Figure 8a shows a whole wafer bonded with 0.4x0.4 mm dies. The dies bonded to the top half of the wafer were saw diced, while the dies bonded to the bottom half of the wafer were plasma singulated. Both groups of dies bonded equally well.

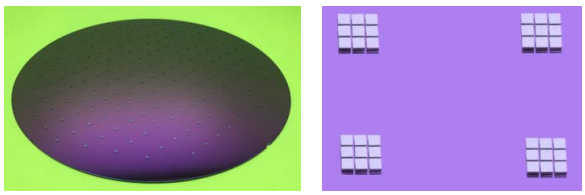
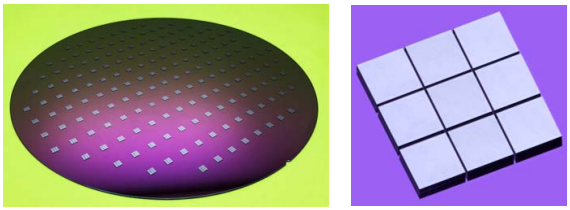


Fig. 8. (a) A 200 mm Blank Si oxide wafer bonded with 0.4x0.4 mm dies. (b) High magnification image of 4 clusters of 9 dies bonded close together to each programed site on the host wafer.

Figure 9a shows a 200 mm blank oxide wafer bonded with 1x1 mm saw singulated die.



(a) (b)

Fig. 9. (a) A 200mm blank Si oxide wafer bonded with 1x1 mm dies. (b) Higher magnification image of a cluster of 9 dies bonded to one programed site on the host wafer.

Table II summarizes the dicing evaluation results through the entire die preparation and bonding cycle. Die singulated with the three techniques, mechanical saw, laser stealth dicing and plasma dicing, performed equally well in the bonding study. Mechanical saw and plasma dicing are suitable for singulation of all three die sizes in this study. Laser stealth dicing can be used for the 3x3 mm and 1x1 mm dies. 0.4x0.4 mm die failed due to poor die separation. Further evaluation is required to assess if the process can be optimized for die of this size.

TABLE II. DICING EVALUATION RESULTS

Die size	Saw dicing	Stealth dicing	Plasma dicing	Die-on-tape prep	Die ejection from tape	D2W Bonding
3x3 mm	Pass	Pass		Pass	Pass	Pass
1x1 mm	Pass	Passs		Pass	Pass	Pass
0.4x0.4 mm	Pass	Fail	Pass	Pass	Pass	Pass

VII. BONDING INTERFACE QUALITY ASSESSMENT WITH DAISY CHAIN DIES

3x3 mm size Daisy chain test dies with the design shown in Figure 3 were processed and bonded. The host wafer used in this case can accommodate 3x3 mm dies only. The dies used in this study were singulated by laser stealth dicing. All dies picked from the dicing tape frame were bonded successfully. The area near the wafer notch was left unbonded on purpose. After D2W bonding at room temperature, the wafer was annealed at 300ºC for 2 hours. Figure 10a shows the whole-wafer image of the very first bonded 200 mm daisy chain host wafer for 3x3 mm daisy chain die. Figure 10b is a closeup image of 8 bonded dies.

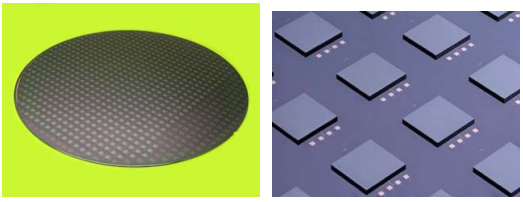


Fig. 10. (a) A 200 mm daisy chain host wafer bonded with 3x3 mm daisy chain dies. (b) A closeup image of 8 bonded dies.

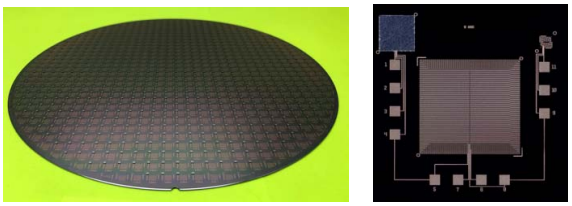
Electrical testing of all three chains showed high electrical yield for this prototype. The yield is calculated as the percentage of die that all three chains passed electrical test.

Table III shows tabulated the results calculated from CSAM and electrical test. 633 out of the 671 die bonded on the wafer are void free, resulting in a 94.3% void-free bonding yield. The voided die are expected to fail electrical test and are excluded from the Cu-to-Cu connection yield. In addition, 9 sites on the host wafer was identified as defective before bonding and were excluded from the electrical test yield calcuation. 603 out of the 624 void-free good die sites showed electrical continuity with the resistance value close to book value, resulting in a Cu-to-Cu connection yield of 96.6% for all the 9488 links on the daisy chain die on the very first wafer bonded. The yield is expected to improve with some fine tuning to the die ejection and bonding processes.

TABLE III. BONDING INTERFACE CSAM AND CONTINUITY TEST RESULTS ON THE 3MM SIZE DAISY CHAIN TEST DIE

Total die bonded	671
Void-free die count	633
Void-free bonding yield	94.30%
Defective die sites on host wafer	9
Good void-free die count	624
Die count passing continuity test	603
DBI connection yield	96.60%

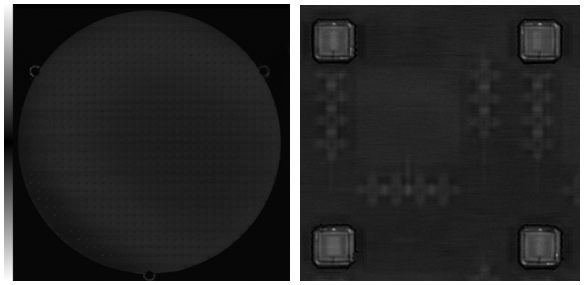
Figure 11a shows a picture of the first multi-size daisy chain host wafer bonded with 1x1 mm daisy chain dies. The dies were saw singulationed. Figure 11b shows a closeup image of one site on the wafer.



(a) (b)

Fig. 11. (a) 200 mm multi-size daisy chain host wafer bonded with 1x1 mm daisy chain die. (b) A closeup image of 1 site on the substrate with the 1x1mm slot bonded.

Figure 12a show the CSAM image of the bonding interface for the entire wafer shown in Figure 11a. Figure 12b shows a closeup image of 4 dies. Well bonded surface shows gray color. The gray color varitaion in the daisy chain area is due to metal trace interference. No void was oberseved in the daisy chain area of the die. The relatively white spots in the center of the top edge and at the corners are due to the die serial number (shown in Figure 3b), bonding fiducials and verniers for measuring die alignment.



(a) (b)

Fig. 12. (a) CSAM Image 1x1mm daisy chain die bonded to a 200mm host wafer; (b) larger image of 4 die showing more details.

Daisy chain continuity was tested. Figure 13 shows the electrical testing result map for all three chains on the die, with a total of 926 daisy chain links on each die. All passing dies are colored green. 751 of the 757 dies bonded passed continuity test. IR microscopy inspection of the failed dies showed all 6 dies have metal pattern defects either on the substrate or on the die. Figure 14 shows an image of a die failed due to missing metal trace for two links on the substrate. Excluding these 6 dies from the yield calculation, electrical connection yield is 100% on the very first lot bonded with this substrate design and 1x1 mm die size.

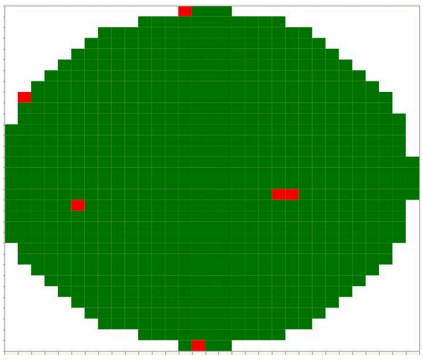


Fig. 13. Daisy chain electrical continuity test yield map for the 200mm host wafer shown in Figure 11. Green: pass; Red: Fail

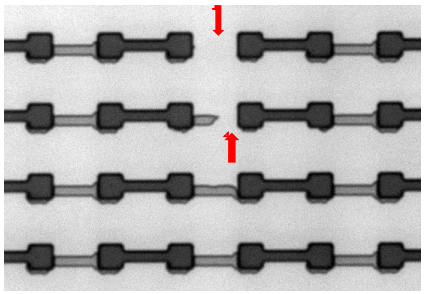
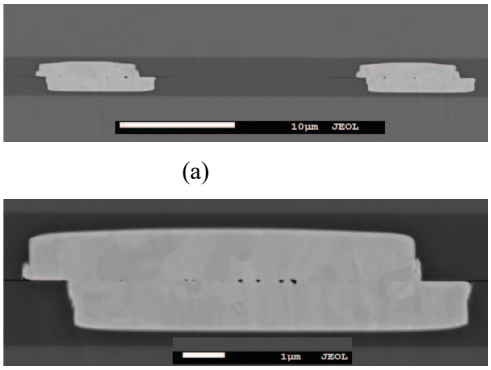


Fig. 14. IR image of a bonded die that failed continuity test. Root cause is the missing metal trace on the substrate as indicated by the right arrows.

Upon completion of electrical test, a die was cross sectioned for the bonding interface quality evaluation. As shown in Figure 15, solid Cu-Cu joints were established. The micro voids at the bonding interface is not expected to impact functional performance or reliability, as shown in our previous publication [9].

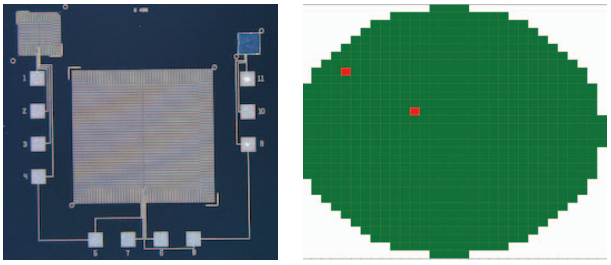


(a)

(b)

Fig. 15. (a) SEM cross-section image of the Cu-Cu joints at the bonding interface, showing good connection; (b) Higher magnification image.

Another 200mm mulit-size host wafer was bonded with 0.4x0.4 mm dies. Figure 16a shows a site on the host wafer bonded with the 0.4x0.4 mm die. Figure 16b shows the electrical testing result map for both chains on the die, with a total of 107 daisy chain links. All passing dies are colored green. 758 of the 760 dies bonded passed continuity test , giving 99.7% test yield.



(a) (b)

Figure 16. (a) A closeup image of one site on the substrate wafer with the 0.4x0.4 mm slot bonded. (b) Daisy chain electrical test yeild map for the wafer.

VIII. DISCUSSION

Hybrid bonding offers many unique features, monolithic Cu-Cu joint, all-solid bonding interface, simple material stack-up, hermetic seal through bonded oxide, zero bond line thickness, and ultra-fine interconnect pitch, to name a few. These features can provide performance advantages such as higher current carrying capability, higher service temperature, reduced parasitic capacitance and inductance, enhanced heat dissipation, better protection against corrosive environments, and thinner profile over traditional packaging techniques for many small form-factor dies.

One type of small form factor package that can benefit significantly from D2W hybrid bonding is a laser diode package, which requires precision alignment in Z direction, high heat dissipation and seal or shielding to prevent contamination in service. Traditional solder interconnect tends to have relatively large height variation (um) making precise alignment very challenging. The zero bond-line thickness of hybrid bonding is ideal for precision Z direction alignment. Direct Cu-Cu bonding enhances heat removal [20], and the hermetic seal by the bonded dielectric prevents ingress of contaminants of the into the package in service.

The demonstration of small die hybrid bonding is promising for realizing widespread heterogenous integration. Bonding of die from multiple type of semiconductor materials and different technology nodes are key to high performance and cost effective heterogenous integration. Many die that need to be integrated are small. This work demonstrate that the small die will not be the bottle neck of such integration.

MEMS packaging would greatly benefit from small die D2W hybrid bonding. It allows easy integration of TSVs for electrical signal through a vertical stack of multiple components through direct bonding of TSV to pads or TSV to TSV, as demonstrated in our previous publication [21].

Small die-on-tape processing has very good value proposition compared to other methods of die preparation. As the die size decreases, the overhead for handling dies individually through picking and fixturing increases. Our HVM die-on-tape process adds no overhead for die cleaning and preparation compared to larger die. Small die D2W bonding also enjoy the enhanced assembly yield, as evident from our data on the 1x1 mm and 0.4x0.4 mm dies. We achieved 99.7% electrical test yield for a 0.4x0.4 mm size 107-link bonded daisy chain dies and 100% test yield for the 1x1 mm size 926-link bonded daisy chain dies on our very first two assembly lots with the new multi-size host wafers.

IX. SUMMARY

The entire W2D hybrid bonding process from wafer grinding and dicing to direct pick & place from a tape frame was evaluated with three die sizes ranging from 0.4x0.4 mm to 3x3 mm.

1) All 3 die sizes 3x3mm, 1x1 mm and 0.4x0.4 mm were successfully bonded with D2W hybrid bonding

2) The performance of three dicing techniques were evaluated for die in this size range. Mechanical saw dicing and plasma dicing are suitable for all three die sizes. Laser stealth dicing is suitable for 3x3 mm and 1x1 mm die.

3) Dies singulated with all 3 dicing methods performed equivalently in the HVM die-on-tape handling process, in preparation for bonding.

4) All three die sizes were successfully ejected from a tape frame and bonded well to the host wafer, with 100% successful die transfer

5) Daisy chain test die with damascene Cu bond pads to a daisy chain host wafers showed good interface bonding quality. Void free bonding yield of 94% and electrical continuity yield of 96% were achieved on the first assembly lot of the 3x3 mm die. 100% void free bonding yield, 100% electrical test yield was achieved on the first assembly lot of the 1x1 mm die and 99.7% electric test yield was achieved on the first assembly lot of the 0.4x0.4 mm die.

In summary, the DBI Ultra die-on-tape HVM D2W bonding process is suitable for small die applications.

X. AKNOWLEDGEMENT

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