Analysis of Die Edge Bond Pads in Hybrid Bonded Multi-Die Stacks

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Abstract— **The Direct Bond Interconnect (DBI®) Ultra technology is a die-to-wafer (D2W) or die-to-die (D2D) hybrid bonding technology that offers high density Cu-Cu interconnect modules using low processing temperatures. Advances in wafer-to-wafer hybrid bonding technology enabled high volume production of backside-illuminated CMOS images sensors [1] several years ago. Continued development of the supply chain and technology enabled manufacturing of D2W hybrid bonded performance compute modules, for example CPU L3 SRAM [2, 3]. The DBI Ultra D2W technology offers a die-on-tape process that meets the needs of high throughput assembly. The value of the DBI technology can be realized across a wide range of devices and form factors including 2.5 and 3D IC stacking. To proliferate this technology in the industry, it is necessary to define design guidelines and understand the influence of processing and layout interactions.**

Hybrid bond pad performance is studied as a function of the proximity to the die edge for single die and multi-die stack configurations. The test structures for multi-die stacking analysis are 8 mm x 12 mm die that contain TSVs on a 35 µm pitch which connect to a 15 µm direct bond pad. The direct bond pad array areas include a die center array with 9,480 direct bond interconnects and edge arrays that contain 315 links per column of interconnect. The eight outermost columns of the DBI pad array extend to 80 µm from the die edge.

Die stacks ranging from 1-8 die are bonded with the DBI Ultra process at room temperature, followed by an anneal at 250°C. The bond interface is characterized with C-mode scanning acoustic microscopy (CSAM) and the interconnect quality is measured through electrical resistance and cross-sectional scanning electron microscopy (SEM). Die bonding configurations include face to face (DBI pad to DBI pad) and face to back (DBI pad to TSV). The electrical test yield and link resistance are presented as a function of distance from the die edge. Additionally, a set of 5-die stacks is subjected to JEDEC standard temperature cycling and high temperature storage tests for comparison between the edge array bond pads and die center array pads. In all design cases, the resistance data showed little dependence on the distance from the die edge beyond 80 µm indicating a minimal width of the peripheral keep-out-zone, which maximizes the area for active DBI pads.

Keywords- Cu-Cu hybrid bonding; design guidelines; die edge; direct bond interconnect (DBI); DBI Ultra; hybrid bonding; D2W; 3D-IC; die stacking; reliability

I. INTRODUCTION

Direct Bond Interconnect (DBI®) is a hybrid bonding technique that is currently being adopted in the semiconductor industry due to its versatility at enabling zero standoff bonding. It is used in a large segment of products such as Back Side Illuminated (BSI) CMOS image sensors and starting to appear in other applications including 3D-NAND [1]. Stacking of die in memory applications is being readied for the market in such products as DRAM and CPU L3 SRAM. [2,3]. DBI technology has many advantages including room temperature bonding, low overall process temperatures, very fine pitch, fully encapsulated copper pads, rapid bonding cycle time, and die-on-tape process flows that enable high throughput assembly platforms. Additionally, there is much work across the industry to integrate TSVs with hybrid bonding to enable true 3DIC stacking. The DBI technology readily bonds TSV-containing die, and in fact DBI pads can be directly bonded onto suitably prepared backside TSV surfaces. This enables surface-to-surface die stacking, as shown in Figure 1.

There are unique topography requirements for direct hybrid bonding since the two bond surfaces have no separation. The dicing process may create local topography issues near the die edge including defects from the die sides and corners due to debris, burrs, and uneven surfaces that can degrade bonding conditions. Degraded bonding can lead to open circuit defects, or possible changes in link resistance relative to the contacts further from the die edge (interior contacts). Because of this, a general practice is to have a buffer region between active DBI bonding pads (those connected to an electrical circuit) and the density change, called a keep-out-zone. Keep-out-zones represent unused die area overhead which generally are minimized or eliminated to reduce cost. Such unused area becomes more of an issue as die dimensions shrink. DBI is a bonding technology that can minimize the size of keep-out-zones.

Double-sided bonding has more complex processing than single-sided bonding primarily due to die preparation and the presence of different bonding structures (DBI-to-DBI for single sided bonding, and the addition of DBI-to-TSV for double-sided bonding). Typically, the backside surface requires additional preparation for bonding, including creation of metal pads that connect to the backside of the TSV such as under-bump metal and copper pillars for solder bumping, or bond pads for hybrid bonding. While stacking multiple TSV die is similar to bonding a single TSV die, it is important to examine yield and performance drivers.

Other factors considered when developing a robust stacking process include maintaining surface cleanliness and high throughput. Hybrid bonding relies on surface-sensitive phenomena, namely surface activation which requires a chemically clean and smooth surface. For commercial viability it is necessary to have a toolset that is widely available and has high throughput. The results presented are based on underlying technical choices that assure widespread industrial deployment and high throughput processes. The bonding throughput used in this study was approximately 900 die per hour, but higher run rates are easily achievable.

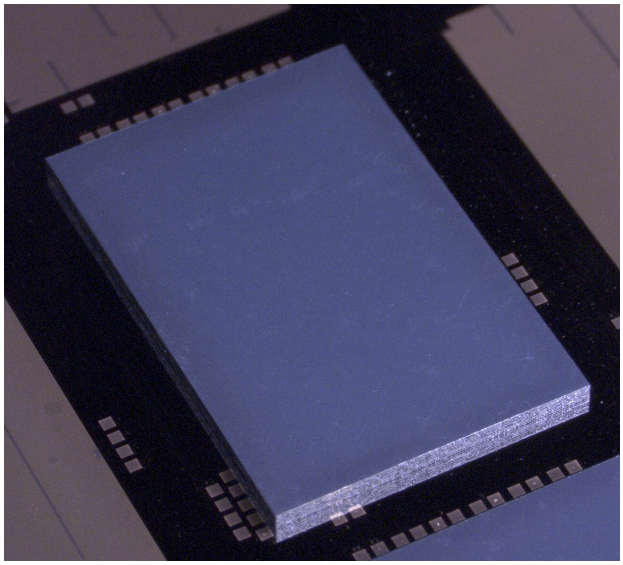

Figure 1. Photograph of a representative DBI bonded 8-die stack.

A special test structure was created with daisy chains that extend to within 85 µm of the die edge. The electrical yield and resistance were measured as a function of the distance of the hybrid interconnect pads to the die edge. Additionally, die stacks with and without TSVs were examined.

II. Experimental Details

A. Device Design (Layout and Cross Section)

The test vehicle was designed to enable flexibility in die stacking. The design has a common host wafer (referred to as Logic, or L), a passthrough die consisting only of TSV and DBI pads (referred to as Thru, or T), and a top die with links to complete the circuit (referred to as Cap, or C). The Thru die is a pass through for the signal, and any number of Thru die (from zero to many) can be stacked. In this study, stacks of one to eight die were prepared using zero to seven Thru die topped with a Cap die. The next section describes how the die fit together. It is possible to get a non-TSV baseline using just a Logic wafer and Cap die (a.k.a. die-to-wafer or D2W stack).

The test vehicle is an 8 mm x 12 mm die that has an assortment of test structures within the middle of the die. The floor plan is shown in Figure 2. The edge array, which was used in this analysis, is located on the left side of the die and is connected with pads 13 through 21, and a large area main array chain is connected with pads 1 through 4.

The DBI pad layout has 15 µm diameter bonding pads on a 35 µm pitch. The RDL nominal linewidth is 10 µm. The 15 µm pad on the front side surface was designed to ensure adequate overlap with the alignment accuracy of the pick and place bonder (±7 µm 3σ). Within the array are daisy chain structures to study hybrid bonding performance, including a main array chain within the center of the die, and daisy chains along the die edge. The main array chain consists of 9450 links that run the length of the die.

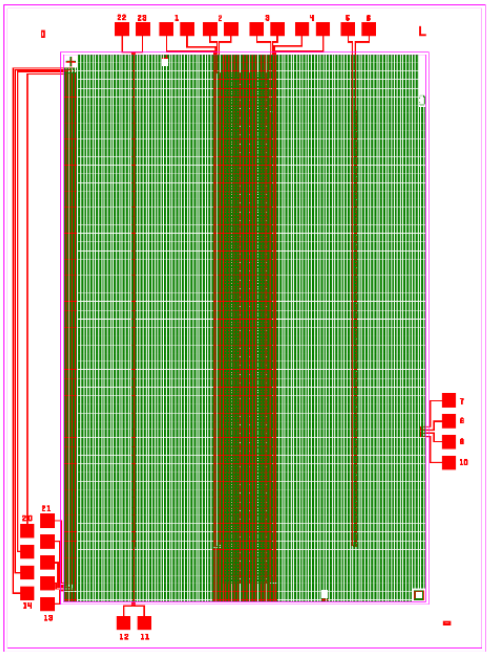

Figure 2. Floor plan layout. The edge array daisy chains are connected to pads 13 through 21 along the left-hand side of the die.

An array along the left edge of the die, made of 8 parallel columns of daisy chains of DBI pads and TSVs, was used to study potential edge effects. Each individual column within the array is connected to different sets of probe pads to enable column-by-column probing. Each edge chain consists of 315 links, and they are connected by links between ends of the columns to form a full array of 2512 links. The outermost and innermost daisy chain columns are about 85 µm and 330 µm from the die edge, respectively. At 330 µm, which is larger than the assumed CMP length scale of 100 to 200 µm, it can be assumed that the topography and thus bond behavior of the innermost column is representative of the interior of the array; measurements of the main array chain provide reference values. Figure 3 shows the detailed edge array connection points for each of the eight daisy chain columns. A corresponding set of probe pads are routed to the far end of the array. Electrical taps on alternating ends make it possible to measure each column.

B. *Device Fabrication*

Figure 4 shows the schematic cross sections of the different die types. Both the Logic and Cap die are fabricated with 2 single-layer copper damascene steps with a 1 µm thick redistribution layer (RDL) and a 2 µm thick DBI layer (see Figure 4a). The Logic and Cap structures were fabricated either on 300 mm wafers at Fraunhofer Institute for Reliability and Micro-Integration (IZM-ASSID) or 200 mm wafers within Xperi's prototyping wafer fabrication facility. The Thru wafers have a similar two-layer metal structure but have 5 µm diameter and 50 µm thick TSVs underneath (see Figure 4b); they were fabricated by IZM-ASSID using a TSV fabrication process that has been reported in detail elsewhere [4].

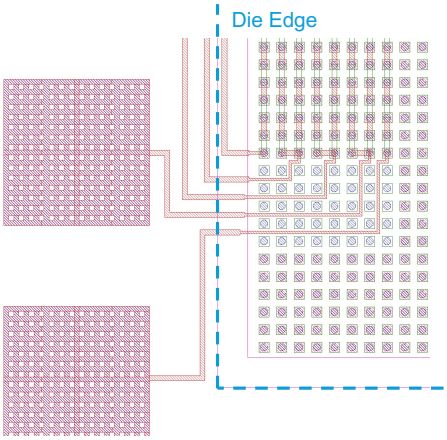

Figure 3. Close-up to edge daisy chain test structure with pads 13 and 15 shown.

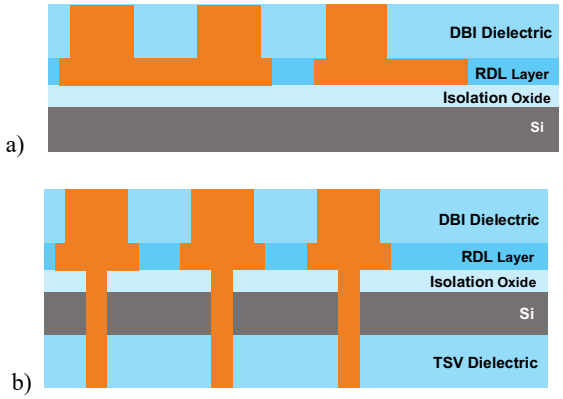

Figure 4. Stack schematics, a) layer stack for the Logic and Cap die, b) layer stack for the Thru die with TSVs. Orange areas refer to copper metallization, light blue areas refer to dielectric.

Error! Reference source not found. schematically shows the orientation of the different components when assembling a stack. The Logic wafer has the DBI surface facing up, while the Thru and Cap die have the DBI surface facing down (therefore the TSV backside is facing up). Both the DBI pads as well as the backside TSV surfaces are processed to have DBI bondable surfaces.

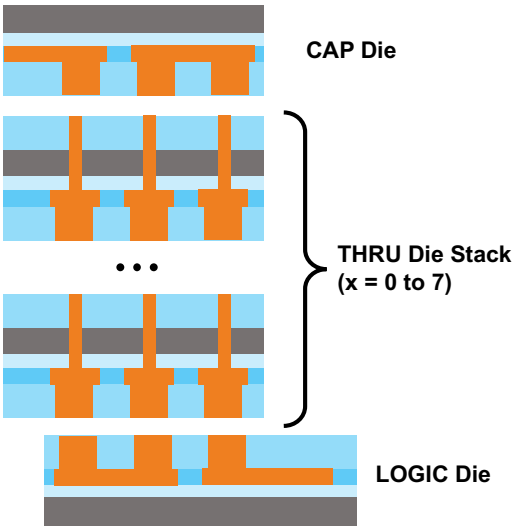

Figure 5. Stack schematic of die stack (LTxC) showing the daisy chain structure.

To construct this structure reliably, several factors should be considered. A key enabling technology for hybrid bonding is careful topography control through device layout and advanced CMP processes. The process is similar to that of single-sided D2W fabrication, provided that both sides of the TSV-containing die meet the same topography requirements. Previously, we reported typical Cu recess variation of less than 3 nm across 300 mm wafers [5, 6]. The CMP process is easily transferrable to commercial equipment from different manufacturers as demonstrated in this study for both 200 mm and 300 mm wafers. The DBI process is capable of handling hybrid bond pad diameters ranging from <1 to 20 µm.

Successful fabrication of DBI-bonded stacks also requires careful management of surface contaminants and particulates. Thru and Cap wafers are converted into thin die before bonding, and contamination control during the dicing and die handling processes can be much more challenging than in the wafer-to-wafer bonding process. To minimize contamination from the die preparation steps after singulation, simplify handling, and make it compatible with high-throughput toolsets, the entire die preparation process is carried out with the die on dicing tape. The bondable surfaces must be cleaned to remove particulates and organic residue without appreciably changing the surface topography.

Cap wafers were thinned to 50 µm, and the backside was not polished as it was not intended to be a bondable surface. For TSV wafers, it is necessary to reveal and prepare the backside surface for DBI bonding as well. The Thru wafers were thinned to 50 µm through a combination of surface grinding, TSV reveal etching, and CMP. This TSV backside surface is directly bonded to the DBI pads of the next layer, as shown in Fig. 5. The significant process simplification here is enabled by a proprietary CMP process on the backside TSV surface that creates DBI-compatible topography. The wafers are then mounted on tape, singulated by stealth dicing, and cleaned. The dies are bonded using a flip-chip bonder.

Maintaining rigorous contamination control protocols is critical in all areas of production from singulation, die transfer,

and bonding to obtain high yield stacks. Assembly work for this study was performed in a class 1000 laboratory cleanroom to minimize particle contamination during die transfer and bonding. The die stack assembly involves a cyclical process flow of cleaning, activating and bonding die in individual layers using a Besi Datacon 2200 Evo plus bonder set to run at a rate of 900 UPH. Bonding was performed under ambient atmosphere at room temperature. Each stack was assembled on a Logic wafer, by stacking zero or more Thru die and placing one Cap die on the top of the stack to complete the circuit. A variety of stacks were made for the study and are denoted LTxC, in which x is the number of Thru die. Thus, an LC means a single D2W, an LTC stack means a single Thru die in between Logic and Cap die for a 2-die stack, and LT7C means seven Thru die to form an 8-die stack. Once stack assembly was complete, the wafer was annealed at 250°C for 1 hour.

Electrical measurements were made using a two-probe system using a single Agilent B1500 SMU and a Wentworth 300 mm probe station with Signatone probers and 5 µm tungsten tips. Multiple measurement passes are made on the wafer, with each pass dedicated to measuring one particular test structure.

To prepare the samples for reliability measurements, the samples had reliability compatible plating over the probe pads on the Logic wafer. The Logic wafer was singulated into individual die stack modules for processing through the tests; there was no encapsulation of the die stack. Time-zero resistance measurement, and CSAM scans of the individual 5-die stack modules were collected. The parts were then grouped for reliability testing. Electrical tests were made on the entire set of chains.

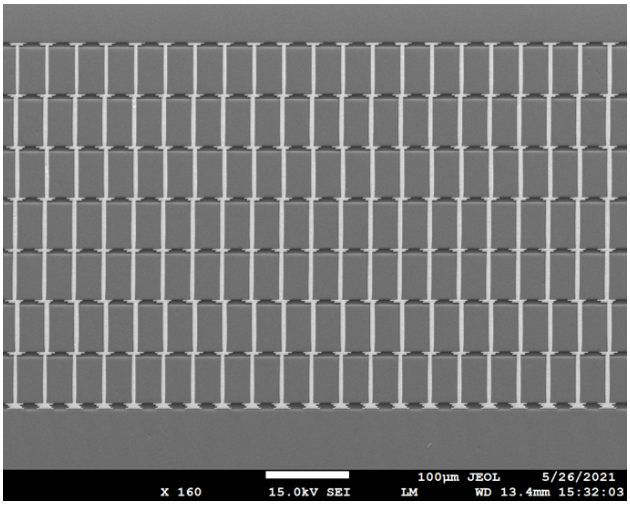

Figure 6. Die cross section of an 8-die stack.

III. Results

A. Die Stack Cross Sections

The DBI hybrid technology has been used to build D2W structures as well as multiple types of die stacks. A SEM cross section of an 8-high die stack is shown in Figure 6. This image shows direct interconnect bonds between seven TSV die and one Cap die. Figure 7a shows a closeup of a single layer within an 8-die stack, while Figure 7b shows a closeup of one of the interfaces indicating that the DBI pad is bonded directly to the backside surface of the TSV. These images show complete copper to copper bonding after the batch anneal.

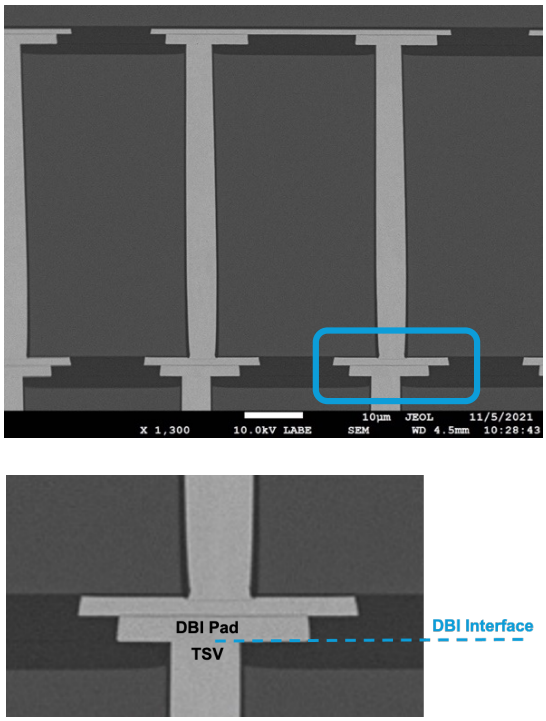

Figure 7. Die cross sections, a) close-up of a single layer within 8-die stack of Figure 6 showing TSVs with DBI bonds, b) close up of a single DBI pad/TSV interface.

B. Void Free Yield

C-mode scanning acoustic microscopy (CSAM) was performed to identify voiding at any die interface. Daisy chain measurements of the parts were made to identify electrical yield and line resistance. The 5-die stacks were subjected to various reliability testing, electrically tested, and lastly examined by CSAM.

Bond void defects can lead to open circuits. Yield loss in this study should mainly be due to voiding or defects, instead of die alignment issues, since bond misalignment was ±5 µm 3σ which is smaller than the DBI pad diameter. Using an optimized die-stacking process, it was possible to achieve a consistent per-layer void free yield for all 5 layers. The void free yield per layer ranged from 85% to 99% (see the points in Figure 8, which averages to 94% yield per layer). However, the cumulative void-free die yield is 73%. While the voids can occur anywhere within the die, they tend to be towards the edge of the die.

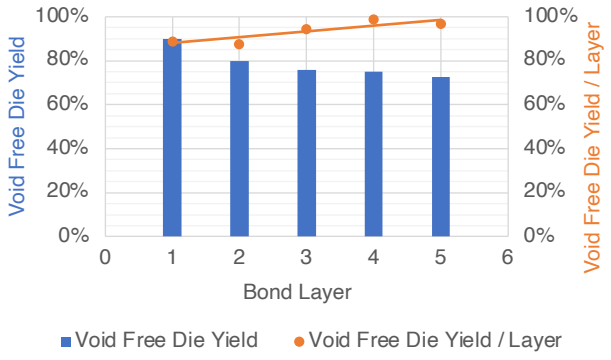

Figure 8. Cumulative void yield of 5-die stack void. The bars indicate cumulative void yield, while the points show per layer void yield. The fitted line is for visual emphasis only.

Figure 9 shows high resolution CSAM images for a single layer D2W bonded die and a 5-die stack to show the location and size of the most common type of voids. High resolution CSAM can also be sensitive to changes in metallization and shows the locations of higher density metal across the surface of the test vehicle. Figure 9a shows the presence of the daisy chains including the edge structure on the far left, while Figure 9b shows the image of a 5-die stack with a typical small void on the opposite side of the die from the edge array.

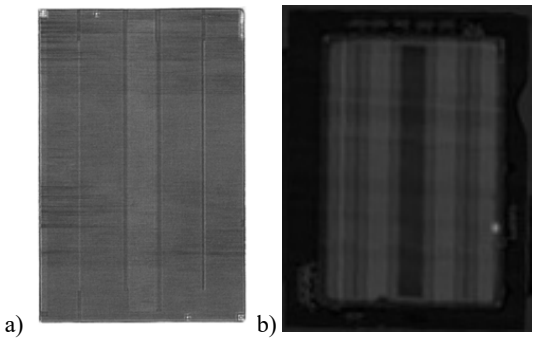

Figure 9. CSAM closeup of example bonded die, a) D2W, b) 5-die stack.

C. Electrical Yield

The electrical yield is shown as a function of distance from the die edge in Figure 10. The data was normalized against the yield of the innermost chain (330 µm). D2W devices show minimal yield loss across the entire array to the outermost chain, with ~100% normalized yield at 85 µm and a minimum of 99% at 155 µm. Figure 11 is a plot of the yield for each column as a function of distance from die edge for D2W stacks, providing a magnified view of Figure 10. Two-die stacks maintain normalized yields in excess of 90% all the way to the outermost chain, as well. However, 5-die stacks fall below 90% electrical yield at 155 µm from the edge and drop to about 28% at 85 µm.

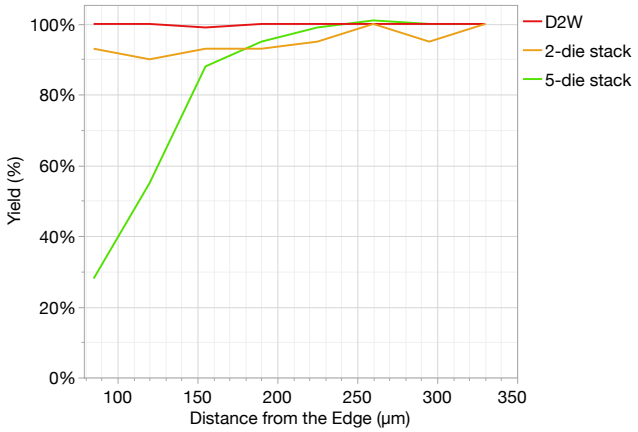

Figure 10. Yield for single chain of different stack heights, normalized to the yield of the innermost chain (330 µm).

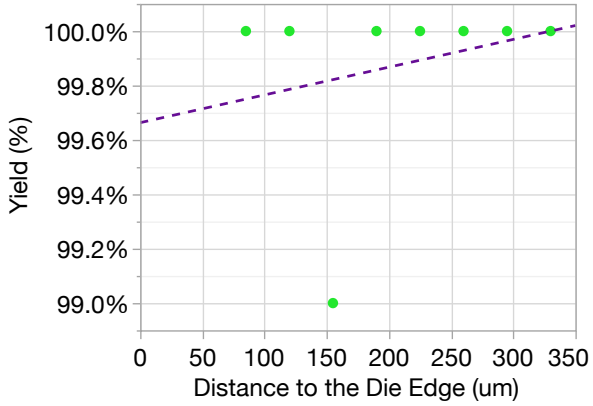

Figure 11. Fit of electrical die yield for D2W stack as a function of distance from the die edge (die N=1213).

D. Link Resistance

To check for any influence of edge proximity to hybrid bond resistance, Fig. 12 shows the complete stack link resistance as a function of distance from the die edge for each stack; the dotted lines show the linear fit. The link represents all components including the RDL links, DBI pads, and TSVs in the Logic and the Cap, and, if present, the Thru die that comprise the stacks. For every stack type, no link resistance dependence with respect to the distance from the die edge is observed.

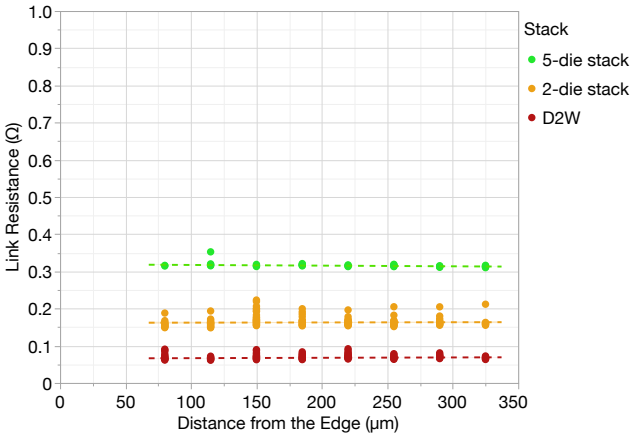

Figure 12: Full stack link resistance as a function of distance from the die edge for each column measured die stacks.

The distributions of link resistance values from yielding stacks are shown in Fig. 13 with the mean value increasing from 0.07 Ω for D2W to 0.32 Ω for 5-die stacks. A link refers to a connection between the link and DBI pads in the Logic and a Cap die along with any TSV and DBI pads in the Thru die. The link resistance excludes any probe pad and lead trace resistance from the measured chain resistance. The sample size is 1213, 308, and 415 for the D2W, 2-die, and 5-die stacks, respectively. The main distribution for D2W contains 96% of the data points, that for 2-die stacks contains 86%, and that for the 5-die stacks contains ~100%.

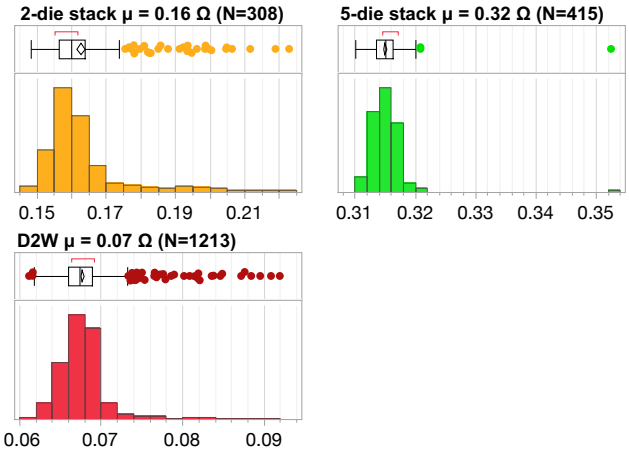

Figure 13. Distribution of average resistance per link for tested chains.

Fig. 14 shows the linear dependence of link resistance as a function of the number of TSV die in the stack. The fit is R_{Link} = 0.0451 Ω + (0.0500 Ω * TSV), with a correlation coefficient of 0.9975. The intercept is the link resistance of the D2W stack, and the slope matches the expected TSV resistance.

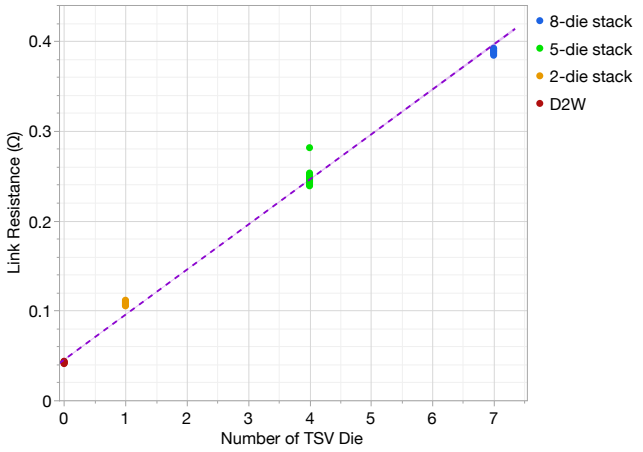

Figure 14: Link Resistance as a function of number of TSV die in the main array chain.

Table I lists the link resistance component of just a Thru die within the stack, which is determined by subtracting the average D2W link resistance value from the chain link resistance and dividing by the number of Thru die in the stack. It compares the mean link resistance from within a layer for the main array at the die center with the innermost (330 µm) and outermost (85 µm) edge array daisy chains. The values for all three stacks fall between 0.049 and 0.066 Ω/layer. There is no substantial difference between the main array resistance and the edge array resistance. Nor is there significant difference in the values as a function of stack height, indicating there is no degradation of interconnect quality.

TABLE I. MEAN LINK RESISTANCE PER TSV DIE LAYER

	Main Array (Ω)	**330 µm Daisy Chain (Ω)**	**85 µm Daisy Chain (Ω)**
8-die stack	0.049	0.064	-
5-die stack	0.051	0.054	0.053
2-die stack	0.066	0.056	0.062

E. Reliability Results

As part of reliability studies carried out on 5-die stack parts based on the main arrays, ancillary data was collected for the edge arrays as well. Discussion and methods for the main array data are found in ref [6]. The sample size for the yielding edge arrays was smaller than the main arrays. The parts were split for the following reliability tests: temperature cycling (TCT), autoclave, high temperature storage (HTS), and moisture sensitivity level 3 (MSL3). Each test population contained parts with yielding edge chains, and all edge chains passed each test. There does not appear to be a reliability failure mode related to DBI pads and TSVs near the die edge.

IV. DISCUSSION

A. Yield

For D2W and 2-die stacks, high-yield is demonstrated all the way to the outermost column of DBI pads that are within 85 µm of the die edge. While taller die stacks also yield near

the edge, there is a yield drop. This drop may be related to edge voids and does not appear to be related to surface topography. Edge voids can occur by a defect-based mechanism such as die edge damage, or bond wave propagation between surfaces [7]. In general, failure probability increases with stack height since adding each layer comes with a certain probability of voiding. Therefore, improvements in the edge yield will be based on understanding the voiding mechanism and accordingly controlling the edge defects or bond propagation.

B. Resistance

Furthermore, interconnects have equivalent performance whether they are near the edge of a die or near the center (Fig. 12). The edge array resistance matches the main array resistance, so there is no difference between die-interior and die-edge interconnects. Also, the link resistance values of edge arrays revealed no significant dependence as a function of distance to die edge. The trend is the same for both D2W and stacked die. Variations are more likely the result of slight changes in probing or lead length correction factors. This demonstrates that DBI bonding out to the array edge does not influence circuit resistance either.

The link resistance of the hybrid bonded interconnect was not affected by the height of the die stacks. No additional interface resistance is added with each layer of TSV interconnect and hybrid bond pad (Fig. 14). The relation between stack height and resistance is linear, and the calculated TSV resistance is ~ 0.05 Ω which is identical to the fit slope. This is critical as it shows that well-aligned hybrid bonding itself does not add resistance to the circuit.

C. Reliability

As mentioned, all edge chains measured for reliability passed their respective tests. Previous reliability work on the main TSV array within this set of parts showed all samples passing [6]. Therefore, the edge array chains show similar reliability to the main array chain.

V. SUMMARY

The hybrid bond interconnect performance was studied as a function of the proximity to the die edge for single die and multi-die stack configurations. High yield (99%) was obtained for bond pads 85 um from the die edge for single die and 2-die stacks (TSV/hybrid bond pad). The 5-die stack showed a dependence of yield on proximity to die edge at 220 μm from the die edge. However, the overall resistance of the DBI links display no dependence on edge proximity or number of stacks. Additionally, the reliability of the edge and main chain connections performed equivalently and passed temperature cycling, high temperature storage and MSL3 reliability tests.

The overall daisy chain yield appears to be defect driven. With careful design and assembly process management to minimize defects, higher stacks are achievable.

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