Elevated Photodiode Arrays
(Monolithic Instruments)

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Integrated Circuit Evolution

First IC
(Texas Instruments)

1st Generation-Simple functions

RTL Flip-Flop
(Fairchild Camera & Instrument)

2nd Generation-Complete electronic systems

CMOS Op-Amp

Microprocessor
(Intel Pentium II)

3rd Generation-Complete instruments

Agilent’s SXGA OLED microdisplay.

Texas Instrument’s DLP © TI 2003

Monolithic Instruments
IC Manufacturing

● 2005 Manufacturing Tolerances
  ● Wafer flatness: < 100nm across a 300 mm wafer.
  ● Metal impurity concentration: < 1 x 1010 cm-3.
  ● Stacking fault density: < 1/cm2.
  ● Layer-to-layer alignment tolerance: < 25 nm.
  ● Linewidth control: 3 nm 3σ.
  ● Minimum feature half-pitch: 100 nm.
  ● Film thickness control: < 4% 3σ over 300 mm.

● 2005 0.25 μm high-volume CMOS device specs.
  ● Transistor Density: ~9 x 107 transistors/cm2.
  ● Operating Frequency: ~1.7 GHz.
  ● Manufacturing Cost: ~ $32/cm2.
    ● Micro-$ 0.36/FET
Value of a Semiconductor Mfg. Platform

<table>
<thead>
<tr>
<th></th>
<th>Semiconductor Mfg</th>
<th>Machining Mfg</th>
<th>Mach./Semi.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Minimum Feature Size</strong></td>
<td>0.25 μm</td>
<td>100 μm</td>
<td>400:1</td>
</tr>
<tr>
<td><strong>Alignment Tolerance</strong></td>
<td>&lt; 25 nm</td>
<td>~ 10 μm</td>
<td>40,000:1</td>
</tr>
<tr>
<td><strong>Manufacturing Cost</strong></td>
<td>$1 \times 10^{-6}$/FET</td>
<td>~$2 \times 10^{-1}$/switch</td>
<td>200,000:1</td>
</tr>
</tbody>
</table>

For the number of devices made, a **semiconductor fab** is the most precise and **least expensive** manufacturing environment.
External Instrumentation Trends

- **Instrumentation**
  - Reduced system size.
  - More computing power.
  - Faster operation.
  - Reduced system cost.
  - Reduced transducer size.

- **Integrated Circuits**
  - Reduced system size.
  - More computing power.
  - Faster operation.
  - Reduced system cost.
    - Improving process control.
    - Improved mfg systems.

Novel solid-state transducers/actuators.

Most instrumentation functions handled by ICs!
Definition of Monolithic Instruments

- Monolithic instruments are miniaturized systems that combine conventional integrated circuits with novel solid-state components that interact with their physical environment.
- Concept: Incorporate several instrumentation system functions onto a single die.
  - Transducer/actuator
  - Driver (analog function)
  - Analog/Digital interface
  - Signal processing
  - Data analysis
  - I/O
Examples of Monolithic Instruments

- Inkjet heads (Hewlett-Packard, Loveland and Corvallis).
- Digital micromirror displays (Texas Instruments).
- DNA microarray detectors (Infineon).
- Direct neuron communicators (Infineon).
- a-Si:H photodiode arrays (Agilent).
a-Si:H Elevated Photodiodes

- Hydrogenated amorphous silicon is a deposited semiconductor.
  - Bandgap ~1.8 eV.

- Advantages
  - Higher QE.
  - Tunable spectral response.
  - Lower thermal effects.
  - Higher fill factor.
  - Cheaper imager.

- Disadvantage
  - Subject to metastabilities that can affect performance (Staebler_Wronski Effect).
Elevated Photodiode Project Roadmap

**Manufacturing**
(Ft. Collins)

**Development**
(Santa Clara)

**Research**
(Palo Alto)

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**1996**
- HP Labs Starts Imager Project

**1997**
- 1st a-Si:H Diode
- 1st Sensor
- HP Labs Informal research project

**1998**
- 1st Product Design Complete
- Interpixel Lkge Sol’n
- Image Lag Solution

**1999**
- Process Freeze
- 2nd PDV complete

**2000**
- Transfer Complete
- SWE Mitigation Project
- Interpixel Lkge Sol’n
- Image Lag Solution
- Dark Current Sol’n

**2001**

**2002**

**2003**

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Elevated Photodiode Array
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Dielectric Isolation Interconnect

- Two extra masking levels.
- Requires a dry etch with high selectivity between two conductive materials.
TFT-Based Monolithic Interconnections

**Fig. 4.12.** Cross-sectional view of a pixel showing the a-Si:H TFT and p-i-n photodiode sensor


**Fig. 4.19.** Example of the design of a high fill factor sensor array using a continuous a-Si:H photodiode layer with a patterned n-type doped contact
Local-via Monolithic Interconnect Structure

Transparent Conductor
p a-Si:H
i a-Si:H
n a-Si:H
Bottom Contact
IC Passivation
Top Conductor Contact

US Patent 6018187
Elevated a-Si:H Photodiodes- Pixel Size Reduction

c-Si 3T Pixel

a-Si:H 3T Pixel
Integrated a-Si:H Photodiode/CMOS Stack

- 0.35 μm 4LM CMOS process.
- 5.9 μm square pixel, on a 7 μm pitch.
- Interpixel isolation created by etching of the n-layer a-Si:H.
- Planarized passivation layer.
a-Si:H Color Sensor Image
(640x480 4.9 x 4.9 µm pixel, 1900 lux)
a-Si:H Material Properties

- Integrated DOS ~2.5 - 4 x 10^{15} cm^{-3}.
- Mid-gap peak ~ 0.88 eV from the conduction band edge.
  - A second peak at ~ 0.83 eV.
- 1.85 eV band-gap.
- E_a ~ 0.9 eV.
- E_U ~ 56 meV.
- Deposition Rate > 30Å/s.

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Effect of p-layer thickness on quantum efficiency

![Graph showing the effect of p-layer thickness on quantum efficiency. The graph plots quantum efficiency (e/photons) against wavelength (nm). Two curves are shown: one for 200A p-Layer and another for 100A p-Layer. The curves reach a peak at different wavelengths, indicating the optimal p-layer thickness for maximum efficiency.]
Effect of layer doping on quantum efficiency

![Graph showing spectral response](image)
Dark Current Components

- Two components of dark current:
  - Junction leakage.
  - Array edge leakage.

- Guardring prevents edge current from reaching the array.

- Sweep guardring and area diode together.
  - Assume: \( I_x = 0 \).
  - \( IE = IA \frac{Aring}{Aarea \, diode} \).
Dark Current Density vs Electric Field

![Graph showing dark current density vs electric field for different current densities (9000A, 7500A, 5500A, 4000A, 3000A). The current density is plotted on a logarithmic scale against the electric field in V/cm. The graph demonstrates an increasing trend with higher current densities.]
Structures and Junction Parameters

- n-layer thickness: 500Å. ([P] 2 x 10^{20} cm^{-3})
- i-layer thickness: 3000 to 9000Å. (5500Å default value)
- p-layer thickness: 200Å. ([B] 7 x 10^{19} cm^{-3})
Effect of Pixel Edge Length on Reverse Bias Current (3000Å I-layer)
Stacked Elevated Photodiode Concept
Integration Challenges

- **Known Issues**
  - Material compatibility with the “nominal” process flow.
    - Adverse effects of the standard structures.
    - Adverse effects of the new structures.
  - Manufacturability of new unit modules.
  - Materials optimization.
    - Material performance considerations.
    - Integration compatibility considerations.

- **Unknown Issues**
  - There will be plenty of them.
  - We encountered 8 major issues in one project.
    - Example: 9 causes of adhesion failure.
Delamination

4 x 4 mm pixel array-
No failure

2 x 2 mm diode-
Bubble failure
Delamination Issues

● 9 adhesion failure modes identified.
  ● Semiconductor interfaces with:
    ● dielectrics.
    ● semiconductor layers.
    ● contacts.
  ● High stress in the intrinsic layer.

● Solutions:
  ● Remove residual contaminants from interfaces.
  ● Prevent methods that incorporate contaminants.
  ● Alter film composition/morphology.
  ● Reduce a-Si:H film stress.
Integration Issue: Blind Spot

- Multiple Issues:
  - CMP WIWNU.
    - Process.
    - Pattern density.
  - Etch selectivity.
  - Dielectric uniformity/thickness.

Pixels OK

Pixels “Bright”

Pixels Dead
SWE Induced Issues

- Artifacts
  - “Fade” - interpixel leakage.
  - “Lag” - increase delay in charge extraction.
  - “Branding” - Localized increase in leakage current.

- Multiple causes
  - Pixel architecture.
  - Layout.
  - Device structure.
  - System level (optics, memory, mechanics).
Interpixel Leakage & Light Shield

- Device measures pixel averages.

Solution: Place metal grid over interpixel region.
- Can maintain superior fill-factor performance.
Image Lag

- Transient photocurrent decay in a-Si:H contributes to image lag in CMOS image sensors. Reduction of image lag improves sensor performance.

- Transient photocurrent reduction techniques.
  - Junction bias.
  - Interpixel bias.

- Mechanism behind transient photocurrent reduction.
Pixel Array Test Device

Side View (Cross Section)

Plan View (Top Down)
Transient Photocurrent Experiment

- LED light focused using prober microscope.
- Optical path fixed throughout the measurements.
- 4156B max. sample rate is 10 samples/second (limiting factor).
- 3488 switching time ~ 1 microsecond.
- HLMP-EP15 capacitance is ~ 40pF.
- Relative measurement.
Effect of Interpixel Bias on Both Pixels

![Graphs showing the effect of interpixel bias on current with different junction biases.](graph.png)
Summary

- Elevated photodiode arrays offer unique advantages for CMOS image sensors.
  - Improved QE, especially at short wavelengths.
  - Tunable spectral response.
  - Unique detector architecture.
  - Less expensive than traditional CMOS imager die.
- Process is robust.
  - Precise manufacturing capability.
  - System integration knowledge is key.
- SWE artifacts can be mitigated.
  - Interpixel leakage solved by grid.
  - Image lag solved by timed reset pulses.
  - Branding solved by:
    - Dark current subtraction.
    - Shutter.