2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding

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***Abstract*— Current DRAM advanced chip stack packages such as the high bandwidth memory (HBM) use through-silicon-via (TSV) and thermal compression bonding (TCB) of solder capped micro bumps for the inter-layer connection. The bonding process has low throughput and cannot overcome the challenge of scaling below 40 μm pitch. These are compelling reasons to seek an alternative approach such as hybrid bonding. The pursuit of fine pitch die stacking with TSV interconnect using hybrid bonding is pervasive in the packaging industry today due to the promise of improved performance. Specifically, the Cu interconnect provides improved thermal and electrical performance and the all inorganic interface of the complete die stack offers enhanced thermal-mechanical performance and reliability in the final chip stack.**

Direct Bond Interconnect technology, also known as low temperature hybrid bonding, forms a spontaneous dielectric-to-dielectric bond at room temperature and then establishes metal-to-metal connection (usually Cu-to-Cu bond) by a low temperature batch annealing process (150 – 300°C). The direct bond process eliminates the need for solder and underfill and associated problems.

While the hybrid bonding exists today in wafer-to-wafer (W2W) format in high volume manufacturing, chip to wafer (C2W) bonding developed for future product lines is making significant process in the past three years. A bonding process with high throughput has been demonstrated with electrical test yield above 90% with a daisy chain structure that covers 50mm² of bonding area. The bonded parts showed superior reliability performance in temperature cycling, high temperature storage and autoclave testing.

This paper presents the latest development in C2W hybrid bonding and demonstrates the low temperature annealing capability and integration with TSV.

Keywords- Cu-Cu interconnect, low temperature, TSV integration, direct bond interconnect, hybrid bonding

I. INTRODUCTION

Requirements for higher I/O density and performance at lower cost is projected to drive the 2.5D and 3D interconnect pitch to 20μm and below. Since the solder interconnect technology faces a fundamental challenge to deliver a high-volume manufacturing solution to meet such requirements [1], the search for alternatives continues. Among the options explored, Cu-to-Cu bonding is considered to be a most promising technology.

Cu-to-Cu bonding can be achieved through two means: Cu-to-Cu thermal compression bonding and room temperature direct bond interconnect, commonly referred to as hybrid bonding.

Cu thermal compression bonding bonds Cu pillars protruded from the dielectric surface. The pads on the opposite side of the device pair to be bonded (C2W or chip-to-chop, C2C)) are held at high temperature (normally 350-400°C) and high pressure to force diffusion of Cu atoms across the interface to form permanent Cu-to-Cu bonding. A common believe was that the high temperature is necessary to destabilize the Cu oxide that forms on the Cu surface at room temperature thereby enabling Cu diffusion across the interface. For applications such as DRAM packaging, the process temperature needs to be under 250°C to avoid degrading the device performance. The majority of research work in low temperature Cu-to-Cu bonding have focused on modification of the Cu surface to achieve bonding temperature reduction.

Panigrahi and Chen reviewed research effort in this area up to 2017 [2]. A large volume of work has been directed to modify the Cu surface prior to bonding to either prevent or reduce Cu oxidation. Methods reviewed include: acid cleaning immediately prior to bonding in vacuum condition; In-situ formic gas environment to reduce Cu oxide during bonding; Organic self-assembled monolayer (SAM) temporary passivation; Ti or Pd layer over Cu for permanent passivation; engineered metal alloy layer for surface passivation, etc. The work cited in the review paper are early stage studies with a single goal of reducing bonding temperature and each method has some disadvantages. The complications include addition of different materials or surface residue, increase in contact resistance, need of vacuum bonding etc.

However, other fundamental challenges for high volume manufacturing (HVM), such as coplanarity of Cu pillars, reliability, and manufacturing cost, have not been addressed. The process relies on metal-metal contact with temperature and pressure, therefore, height compensation

2377-5726/19/$31.00 ©2019 IEEE
DOI 10.1109/ECTC.2019.00100

in traditional solder joints is no longer available. Solder joints can compensate for total thickness variation (TTV) of a few microns to tens of microns, depending on the solder volume and interconnect pitch. For direct Cu-to-Cu bonding, the TTV requirement drops by 2 orders of magnitude to the nanometer range. Traditional Cu bump plating technology cannot meet such requirement, making the technology fundamental unattractive. Second, exposed fine Cu pillars are prone to oxidation and corrosion and encapsulation technology of such joints has not been developed. Finally, a bonding process that requires precision alignment and long bonding time under heat and pressure means low throughput from high cost bonders and is inherently expensive.

Direct Bond Interconnect (DBI) technology, also known as low temperature hybrid bonding [3, 4, 5], has distinctive advantages over thermal compression bonding. This technology bonds metal pads slightly recessed from the surrounding inorganic dielectric (oxide for this study) surface. The bonding is a two-step process. The first step forms a dielectric-to-dielectric bond (SiO_2-to-SiO_2 for this study) at room temperature and then the second step establishes metal-to-metal connection (usually Cu-to-Cu) through a batch annealing process (150–300ºC). Since oxide bonding takes place at room temperature, Cu oxidation during bonding is not a concern. The bonded dielectric layer surrounding the Cu interconnect encapsulates the joints from environment in the annealing oven; thus minimizing Cu oxidation during the anneal process. The bonded oxide surface also hermetically seals the Cu interconnect during device operation.

The technology was first commercialized in wafer-to-wafer (W2W) bonding applications. Since the process bonds two dielectric surfaces at atomic scale, the key challenges for W2W bonding are sub-nanometer surface roughness, surface with low level of contamination, and precise control of Cu recess on the bonding surfaces. A well-controlled chemical mechanical polishing (CMP) process can solve the above challenges. In fact, wafer-to-wafer (W2W) direct bond interconnect technology has been in high volume manufacturing for several years for pad size up to 3µm diameter [6].

The hybrid bonding technology is also ideally suited for high volume chip-to-wafer (C2W) and chip-to-chip (C2C) assembly. Since the dielectric bond process is spontaneous, it has the same speed as die pick and place and is therefore well suited for high throughput. The batch anneal to achieve Cu-Cu interconnects is also acceptable for high throughput volume manufacturing. Extending the technology to the C2W application involves solving some additional challenges. For C2W applications, a larger pad size is desirable to accommodate the alignment accuracy available in HVM die bonder to maintain low assembly cost. Current technology for flip chip bonder can achieve alignment accuracy in the 1-10 µm range. The lower accuracy machines can meet much higher throughput requirements than the high accuracy models. Wafer singulation is also a dirty process; therefore, maintaining a clean die surface for bonding is challenging.

In our previous publications, we have reported development of a high-volume production-ready C2W hybrid bonding process [7, 8, 9, 10, 11]. We have demonstrated C2W bonding at a 10µm pitch with electrical test yield up to 92% of the die on wafer have 100% of the daisy chain covering a 50mm^2 area fully connected. We have also demonstrated a process for cleaning and activating die on a dicing tape in a dicing frame. We then picked die directly from the dicing frame for bonding and have demonstrated throughput of 1636 die per hour with a single head bonder.

We have also demonstrated superior reliability in environmental stress tests including temperature cycling, high temperature storage and autoclave testing. All parts showed superior performance with no increase in resistivity, no crack initiation or defect growth. We have also demonstrated of a 20-die stack with hybrid bonding. The parts shown in the previously published work were annealed at 300ºC. This paper presents the continuation of our hybrid C2W bonding development effort for low temperature applications.

II. Test Vehicle Design and Fabrication

Two different designs were used for this study. Design A shown in Fig. 1 is a daisy chain die of 7.96 mm x 11.96 mm. This die size was chosen to mimic an HBM DRAM die foot print. It has Cu bond pads embedded in SiO_2. Its fabrication includes two Cu damascene processes for the two metal layers. The image shown in Fig. 1 includes a bonding layer, which consists of circular 10 µm diameter Cu bond pads embedded in silicon dioxide, and a Cu trace layer in the shape of a grid for daisy chain connection. Since the oxide is transparent, both layers of metal are visible in the optical image. The daisy chain pitch is 40µm. This design can tolerate 5µm misalignment for assembly.

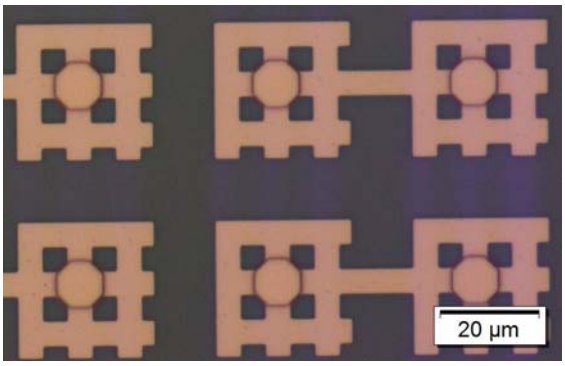


Figure 1. Design A: Daisy chain test vehicle top-down optical image.

The mating die size on the host wafer is larger in the x-axis to accommodate the probe pads for resistance measurement. The host wafer is 200mm size. Test areas on the bonded D2W structure are shown in Fig. 2. The main daisy chain in test area 1 has 31356 links and covers 50mm^2 of bonding area. Daisy chain continuity results reported in this paper are from this test area.

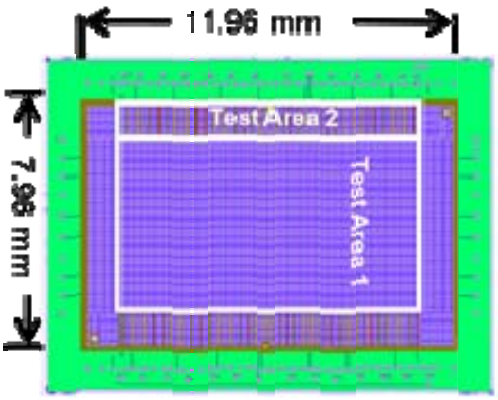


Figure 2. Design A daisy chain test vehicle test areas illustration.

The design B has a single metal layer with 10 µm diameter circular bond pads embedded in oxide with a pitch of 56 µm, as shown in Fig. 3. The mating part is a TSV test vehicle with 10 µm TSV array mirroring the Cu bonding pads shown in Fig 3. Both the TSV wafer and single metal wafer were fabricated by Fraunhofer Institute for Reliability and Micro-Integration, IZM – ASSID. The process for the TSV fabrication has been reported in detail elsewhere [12]. Both the TSV wafer and the single metal wafer for this design are 300mm in diameter.

The hybrid bonding process requires the oxide surface roughness to be less than 1nm. It also requires shallow and uniform Cu recess for low temperature anneal. For bonding pads of 10 µm diameter, most CMP processes used in the BEOL fabrication create Cu recess too deep for low temperature anneal. Xperi has developed a special CMP process to produce shallow and uniform Cu recess [8, 10, 11]. The process was developed on a commercial 200mm CMP tool and transferred to Fraunhofer. The special CMP process scaled well to the 300mm CMP tool and was used for the final surface finish of the 300mm wafers used in this study.

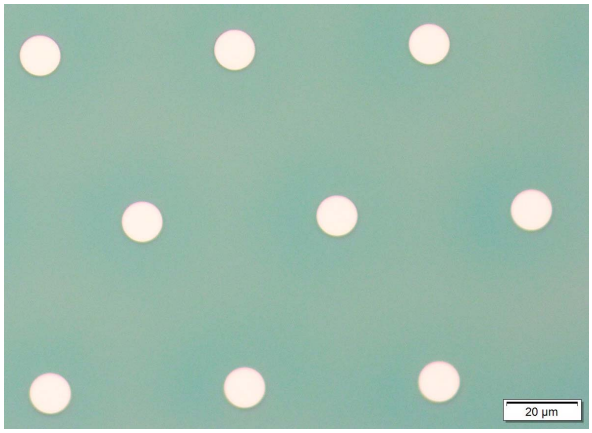


Figure 3. design B test vehicle top down optical image: 10 µm circular bonding pads with 56 µm pitch.

III. WAFER AND CHIP PREPARATION FOR BONDING

The last step of wafer fabrication process is a CMP process to condition the surface to meet the oxide roughness and Cu recess specification for hybrid bonding. The wafer surface after CMP is clean. A rinse in de-ionized (DI) water and a plasma treatment complete the host wafer preparation process.

The wafer used to generate chips for bonding must go through the dicing process. The process generates particles, contaminants, and edge defects. Chip handling during preparation also adds contamination if the process is not well designed and controlled. We applied a protective coating to the wafer surface prior to singulation. After the singulation, the coating is removed with a wet chemical process while the chips are still on the dicing tape. To minimize contamination from the chip preparation steps, the entire clean and preparation process is carried out with the chips on dicing tape. Such process is also well suited for low-cost high-volume manufacturing. Fig. 4 shows a diced wafer at the completion of chip preparation step and is ready for bonding.

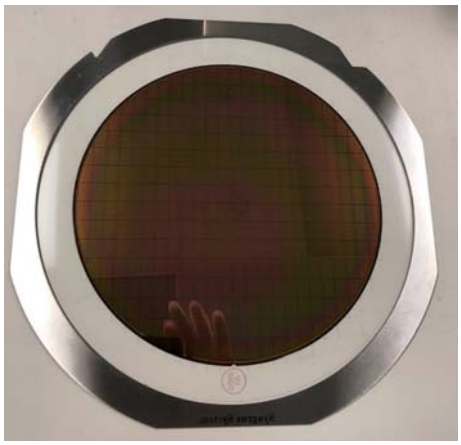


Figure 4. Picture of a diced wafer ready for C2W bonding.

IV. CHIP TO WAFER BONDING

We used a Datacon Evo 2200 machine to pick and place chips from the dicing frame shown in Fig. 4. Bonding takes place in a 1K clean room ambient environment. The host wafer stage is also at room temperature. The process is similar to a standard flip chip pick-and-place process without a flux dipping. Spontaneous bonding takes place as soon as the die surface touches the wafer surface. The bonding process can run at the designed speed of the bonder. The alignment accuracy specification of the Datacon Evo 220

bonder is +/-7µm. We slowed the machine down to achieve better alignment accuracy of +/- 5um on the two designs shown in Fig.1 and Fig. 3. We have demonstrated 1636 unit per hour with our single head machine. This is much faster than the thermal compression bonding process for solder capped micro bumps.

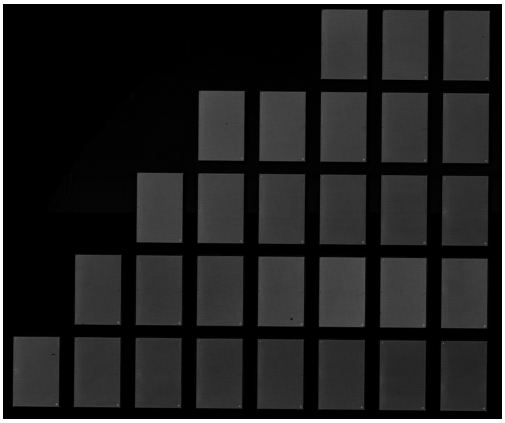
For the design A samples, after population of the entire host wafer with desired number of chips, the wafer was cleaved into 4 quarters for an anneal DOE at various temperatures. The anneal process was carried out in a convection oven. Post-anneal samples were characterized by co-focal scanning acoustic microscopy (CSAM) to check for bonding interface voids. Resistance measurement was carried out to determine full continuity joints between the bonded C2W pairs. Representative bonded C2W samples were also cross-sectioned for examination of Cu-to-Cu metallurgical bond interface.

For design B, the C2W samples were examined by cross-section after annealing.

V. RESULTS

Fig. 5a shows a CSAM image of a Design A sample piece after it was annealed at 200°C for 2 hours. All 29 C2W pairs on the sample piece showed no unexpected voiding. The small white dots at the opposite corner of each chip were voids caused by the fiducial marks used for the C2W bonding. These small voids are stable through reliability testing and do not grow.

Fig. 5b is the resistance measurement results for the same sample piece from the test area 1 shown in Fig. 2. This test area covers 50mm^2 of bonded surface and has 31356 daisy chain links. A "pass" during the electrical test means all 31356 bonding interfaces in the chain are electrical connected. All 29 C2W pairs on the test piece passed the electrical test. The 100% correlation between the CSAM and electrical measurement data is a good confirmation that the 200°C anneal is sufficient to form Cu-to-Cu bonding.



(a)

					Pass	Pass	Pass
			Pass	Pass	Pass	Pass	Pass
		Pass	Pass	Pass	Pass	Pass	Pass
	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

(b)

Figure 5. (a) CSAM image of representative Design A C2W bonded sample after 200°C/ 2 hour anneal. (b) Dasiy chain resistance measurement results of the same sample piece for test area 1 shown in Fig. 2 with 31356 links.

After the experiment with 2 hour anneal at 200°C, we have shortened the anneal time at 200°C to 1 hour for multiple sample pieces from multipe assembly lots spanning a couple of months. As shown in Table 1, 4 out of the 5 sample pieces showed 100% electrical test yield on void free C2W pairs. One sample set showed electrical test yeild of 92%. This result is very encouraging.

TABLE I. ELECTRICAL TEST RESULTS OF DESIGN A SAMPLES ANNEALED AT 200°C FOR 1 HOUR

Build	Sample ID	Anneal Temperature (C)	# Die Pass/# Die No Defect	% Yield
1	#1-1	200	24/26	92
2	#2-1	200	20/20	100
3	#3-1	200	19/19	100
3	#3-2	200	13/13	100
3	#3-3	200	15/15	100

We have also cross sectioned representative samples from each build to examine the Cu-to-Cu interface quality. Fig. 6 shows a cross-section image from sample #1-1 in Table 1. The misalignment between the top and bottom cu pads is within 5 µm. The overlapping Cu surfaces showed no visible gaps between the top and the bottom Cu

bonding pads indicating good electrical bonding. The electrical resistance was very close to theoretical resistance and was statistically equivalent to resistance measured on test samples annealed at 300°C.

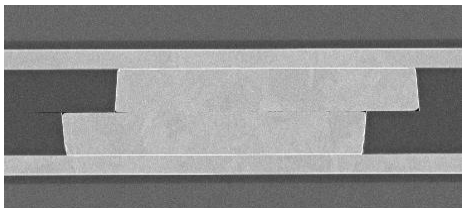
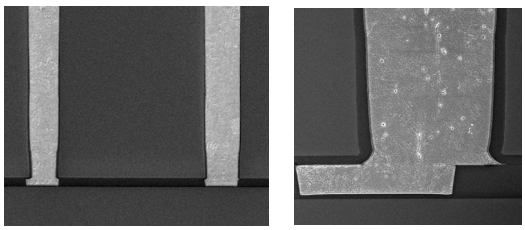


Figure 6. Cross-section image of a sample from build #1 in Table 1 showing good Cu-to-Cu bonding.

We have collected some preliminary results from the Design B test vehicle. Fig. 7 shows a cross-sectional image of a Cu-to-Cu interface between the single layer metal pads and TSVs after 200°C anneal for 1 hour. The approximately 5 μm misalignment between the Cu pad on the bottom and the TSV on the top was due to the limited alignment accuracy of the Datacon Evo 2200 bonder used for the assembly. Despite some micro voids at the interface, a quality Cu/Cu interconnect is achieved.



(a) (b)

Figure 7. Cross-section images of a hybrid bonded C2W sample from the Design B TSV test vehicle annealed at 200°C for 1 hour. (a): Lower magnification showing bonding interface of two TSVs to pads; (b) at Higher magnification image showing the bonding interface of a single TSV to pad.

VI. DISCUSSIONS

The hybrid bonding is a two-step process that includes a dielectric-dielectric instantaneous bond at room temperature, followed by a heated batch anneal process. During the batch anneal process, the Cu features (either Cu pads or TSVs) expand more than the surrounding silicon oxide due to the large differential of coefficient of thermal expand (CTE) between the two materials. Due to the confinement of the oxide, the Cu expands directionally at the free surface and physically bridge the small gap between the two surfaces that exists at room temperature after the oxide-to-oxide bonding. Once the two surfaces are in physical contact, Cu atoms diffuse across the interface to form permanent metallurgical bond. Once the Cu-to-Cu bonding is formed, it will not separate when the part is returned to ambient temperature.

The theory behind Cu-to-Cu thermal compression bonding is: Cu oxide formed at room temperature acts as barrier layer for Cu diffusion during Cu to Cu bonding. It is a common believe that by heating the Cu surface to above 200°C, the Cu oxide formed at room temperature becomes thermodynamically unstable, allowing Cu atom to diffuse through for successful grain growth. However, we believe that the impact of Cu oxides formed at room temperature is highly exaggerated since Cu oxides at much lower rate at room temperature than at elevated temperature used for thermal compression bonding. Keil, Lützenkirchen-Hecht and Frahm have shown that Cu oxide thickness formed at room temperature is a two-layer structure with an outer CuO layer of approximately 1.3 nm thickness and an inner Cu_2O layer of about 2.0 nm [13], giving a total oxide thickness of approximately 3nm. However, according to Lee, Hsu and Tuan, oxidation thickness reached 150 nm after only 1 minute at 200°C and 300nm after only 1 minute at 300°C when exposed to an atmospheric oxygen environment [14]. Clearly, the oxide formed at room temperature at the Cu surface is not the main barrier for Cu diffusion during the bonding process, but rather oxidation at elevated temperature is more likely the root of the problem.

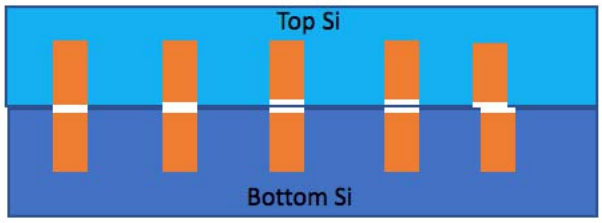
For the hybrid bonding technology, the Cu features to be bonded are completely surrounded by bonded oxide surface at room temperature and isolated from oxygen and/or other oxidizing agents completely. During the heated anneal, a Cu-Cu metallurgical bond is formed as the differential thermal expansion between the Cu and surrounding oxide is sufficient to bridge the gap between the two Cu surfaces and form a compression force at the interface. Additionally, the thin oxide formed at room temperature does not impede the Cu inter-diffusion and the formation of a strong bond. This explains why 200°C one hour anneal is sufficient to form solid Cu-to-Cu bonding.

The large electrical chain in Design A fully exercises the hybrid bonding technology. The longest daisy chain on a die covers an area 5.36 mm x 9.36 mm (50mm^2) and has 31,356 links. By comparison, the HBM2 DRAM design has only approximately 4,000 interconnects between dies covering an area of 0.8mm x 6.1mm (4.9mm^2) in the center strip of a die. As shown in Figs. 5a & 5b, we achieved 100% void free bonding and 100% electrical connection on this test piece. Other lots shown in Table I that were annealed at 200C for 1 hour also showed electrical test yield around 100%.

The key to the void free bonding is a well-controlled clean chip and wafer surface prior to bonding. We have developed processes to clean the chips sufficiently to routinely achieve >90% void free bonding in a prototype environment. The key to high electrical test yield is the uniform Cu recess in the final CMP process. As shown in our previous publication, we have developed a CMP process to produce a Cu recess variation of ≤2.5nm across the entire 200mm wafer [8, 10], a distinctive advantage of the hybrid bonding over the thermal compression bonding.

As illustrated in Fig 8a, for hybrid bonding, the oxide surface defines the plane of bonding interface while the total thickness variation (TTV) of Cu pads is the recess depth of Cu pads from the oxide surface. With the special CMP technology that we have developed, we control the Cu recess variation across the entire wafer to be less than 3nm. For any given C2W pair, the sum of TTV on the wafer side and the chip side will be less than 6nm.

In contrast, The TTV of Cu pillars across a wafer is on the order of several µm. Fig. 8b illustrates the TTV of Cu pillars in thermal compression bonding. The Cu pillars protrude above the oxide surface and the height of Cu pillars is defined by the thickness of the plating resist and electroplating uniformity. A process variation of a few microns across a wafer is common. Although TTV can be reduced by a mechanical planarization process, it is still in the micron range. One publication showed TTV of 1.3 µm across a 300mm wafer after fly cutting [15], which is several hundred times larger than what is achieved in hybrid bonding through CMP. Without a compliant layer (such as a solder), or a soft metal that can deform easily, it is challenging to achieve high assembly yield for large I/O count applications with such a large TTV.



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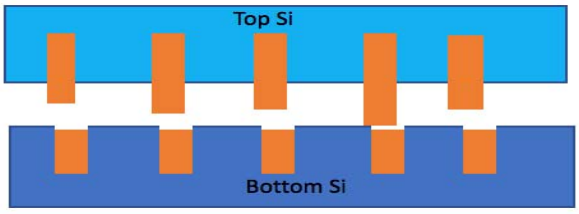


(b)

Figure 8. (a) illustration of Cu pad TTV in hybrid bonding. The TTV is the sum of Cu recess variation across the die, shown as the white gap between the Cu pads embedded in the oxide of the top and bottom die; (b) Illustratio of Cu pillar TTV in thermal compression bonding.

For die stacking applications such as high-performance DRAM, Cu thermal compression bonding faces more fundamental challenges than just the high TTV from electroplating process.

Currently, a temporary bonding technology using a spin coated polymer layer is commonly used for the backside processing of a thin wafer. TTV of 1-3 µm is inherent in the spin coating process. Consequently, the thinned wafer will have 1-3 µm TTV in the best case. After wafer singulation, the worst case TTV for each die is the total sum of wafer thickness TTV and Cu pillar height TTV. For die stacking, the TTV also accumulates through the stack. The die thickness of current stacked package is around 50 µm, the technology development trend is to reduce die thickness further to increase die count in a stack which will further exacerbate the problem.

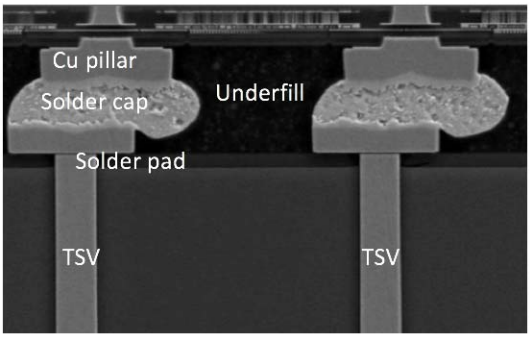
In addition, bonding each layer requires substantial time under temperature and pressure. The first die in the stack will see multiple heating cycles that can significantly degrade device performance. There has been research effort to use a layer of patterned organic materials to glue the die together before the thermal compression process to form Cu-to-Cu bonding. However, the organic material can flow into the gap between Cu features to be bonded during the bonding process and interfere with Cu-to-Cu joint formation.

In comparison, hybrid bonding for the die stacking application is straightforward. Since the TTV for Cu-to-Cu bonding is defined by the sum of Cu recess on both sides of the bonding surface, the die thickness TTV resulted from the temporary bonding process has no impact. Further die thickness reduction increases the flexibility of the die and actually improves hybrid bonding yield. In addition, the two-step nature of the hybrid bonding process is ideal for die stacking application. The oxide-to-oxide bonding which occurs spontaneously at ambient temperature is strong enough to hold the die in place with no additional force. As a result, only one anneal process is required to form the Cu interconnect through the entire stack.

Integration of chip with TSV for stacking using hybrid bonding is also straightforward. Fig. 9a shows a typical solder capped micro-bump thermal compression bonding joint taken out of a System Plus Consulting's report. Multiple lithographic and electroplating steps are required to form a solder pad on the TSV side of the bottom Si and Cu micro bump with solder cap on the device side of the

top Si. These processes increase manufacturing cost. In addition, assembly throughput is low and requires underfill. Fig. 9b is an illustration of the configuration used in the Fig. 7 of C2W bonding with TSV. Compared to the solder capped micro bump TCB process, the following steps are eliminated: 1) fabrication of solder pads in the bottom Si with TSV; 2) multiple step plating process to form the under bump metallurgy (UBM), Cu pillar and solder over the Cu pillar. Instead, a single damascene process is used to form the Cu pads embedded in a dielectric layer (oxide in this study).

Elimination of the solder and underfill from the joint simplifies the process and reduces cost. Additionally, it eliminates the formation of brittle intermetallic compounds and warpage due to CTE mismatch between the silicon and underfill. These two factors are the largest driving force of solder joint crack initiation and growth. We have shown superior reliability of C2W bonded parts without any TSV [10,11]. Work is continuing to demonstrate reliability of parts with integrated TSVs.



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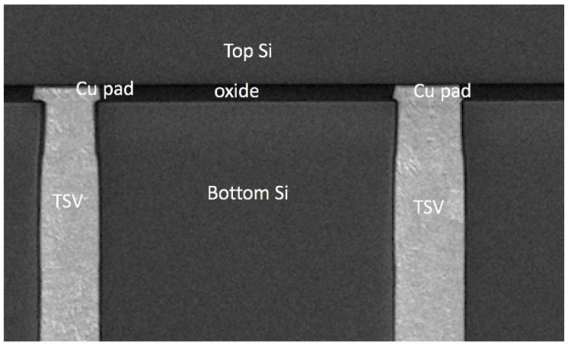

(b)

Figure 9. (a) Typical Cross-section image of a die with TSV joined to another die using solder capped Cu micro bump from a System Consulting's report. (b) Cross-section image of Cu-to-Cu joints in a C2W sample formed by hybrid bonding, demonstrating joint simplificationm.

VII. CONCLUSIONS

The low temperature direct bond interconnect technology promises to enable generations of interconnect pitch scaling below 40 µm. We have demonstrated a C2W technology suitable for applications with 200°C anneal temperature restriction. A daisy chain chip with a test area covering 31356 links and 50mm^2 surface area has been assembled with 1 hour of anneal at only 200°C. Electrical testing of void-free die has showed 100% of the links were connected. SEM images of the cross section showed a solid Cu-Cu metallurgical connection across the bonding interface.

Integration of TSVs into the C2W bonding has also be demonstrated. The fabrication process to form a Cu bonding layer on one side of the bonding surfaces represents major simplification compared to fabrication of solder pads solder capped micro-bumps required to achieve 40 µm pitch with the micro bump thermal compression bonding technology.

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