Chip to Wafer Hybrid Bonding with Cu Interconnect: High Volume Manufacturing Process Compatibility Study

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ABSTRACT
Solder reflow technology is volume manufacturing ready to an interconnect pitch of about 60um for two main reasons. Solder has the ability to compensate for height differences among the interconnects on a die or package through the melting and re-solidification process. The second reason is that pick-and-place tools combined with mass reflow process offer an extremely high throughput and low cost process. Unfortunately, this technology appears to be limited to a minimum pitch of 40 μm. Therefore, the industry is searching for a solid state bonding technology to enable further pitch scaling. The candidate technology should have the following key attributes: 1) a mechanism to precisely control the metal height variation to prevent open joints, 2) high assembly throughput; 3) low temperature for certain applications; and 4) a pathway to future generations of pitch scaling.

DBI® Ultra is a die to wafer (D2W) Direct Bond Interconnect (DBI®) technology that utilizes D2W low temperature hybrid bonding to achieve all of the attributes listed above. It offers precise Cu height variation control through the chemical mechanical polishing (CMP) process. With an extremely efficient pick and place process for assembly, it has a throughput comparable to the solder flip chip reflow process. A spontaneous dielectric-to-dielectric bond at room temperature with a metal-to-metal connection (usually Cu-to-Cu bond) by a low temperature batch annealing process (150 – 300ºC) is attractive for heterogeneous integration. Ultimately, it can scale to a sub-micron pitch.

In the past two years, significant progress has been made in the DBI Ultra technology. A bonding process with high volume production throughput has been demonstrated with electrical test yield above 90% with a daisy chain structure that covers 50 mm^2 of bonding area. The bonded parts also showed superior reliability performance in temperature cycling, high temperature storage and autoclave testing.

This paper demonstrates the low temperature anneal capability of the technology and presents the detailed comparative analysis of the technology against the competing solid Cu-to-Cu thermal compression bonding (Cu-Cu TCB) process.

Key words: Cu-to-Cu bonding, hybrid bonding, DBI® Ultra, D2W, D2D, chip to wafer, die stacking, 3D, 2.5D

INTRODUCTION
Solder flip chip technology was first introduced in the 1960s and has enabled many generations of interconnect pitch scaling[1]. Now the technology is reaching its pitch scaling limit. Above 60 μm pitch, the low cost and high through-put mass reflow process is mature. Fine pitch below 60 μm requires thermal compression bonding of the solder capped Cu micro bumps (TCB μbump), which is much higher cost process with lower through-put. Even with this complex technology, the pitch is stalled at approximately 40 μm for several years already. Further pitch scaling requires the industry to move to an all-solid interconnect technology. Among the options explored, Cu-to-Cu bonding is considered to be the most promising technology.

Cu-to-Cu bonding can be achieved through two means: either Cu-to-Cu thermal compression bonding (Cu-Cu TCB) at elevated temperature and pressure, or room temperature direct bond interconnect (DBI), a low temperature hybrid bonding process.

Cu-Cu TCB bonds Cu pillars protruded from the dielectric surface of one device to Cu pads on a wafer or a second device surface. The pads on the first device match those on the second die to be bonded and are held at high temperature (normally 300-400ºC) under high pressure to force diffusion of Cu atoms across the interface to form permanent Cu-to-Cu bonding. Since Cu does not melt at the bonding temperature, the process

relies on deformation of the Cu pillars and pads to compensate for height differences. High temperatures soften the Cu and make deformation easier while increasing surface self-diffusion. For example, increasing the bonding temperature from 150ºC to 300ºC increases surface self-diffusion of Cu by at least 20 times[2]. However, Cu oxidizes quickly at such temperatures. Thus the bonding process normally requires vacuum, inert or a reducing gas environment. Bonding times of 15-60 minutes is required for reliable bonding.

The Cu pillar for Cu-Cu TCB is normally fabricated by electroplating of Cu into holes defined by a patterned photo resist layer. This plating process normally gives rise to a Cu height variation of several microns across a wafer. Reducing the Cu height variation to the nanometer range is required in order for this technology to be high volume production worthy.

Attempts to reduce Cu pillar height variation by fly cutting with a diamond bit has been reported but appears to be inadequate[3]. Detailed analysis will be given later in the paper.

For applications such as DRAM, the process temperature needs to be under 250ºC to avoid degrading the device performance. The majority of research work in low temperature Cu-to-Cu TCB has focused on the modification of the Cu surface to achieve bonding temperature reduction. Panigrahi and Chen reviewed research efforts in the surface modification of Cu through 2017[4]. All the work cited is early stage proof-of-concept type with small sample sizes. Every method reviewed has some shortcomings such as: Requires bonding in vacuum, which is high cost and not appealing for high volume assembly; CMOS incompatible; high temperature and pressure degrades device performance. The two successful fine pitch Cu-Cu bonding applications cited in the paper: the Sony CMOS image sensor[5] and the Tezarron's 3D DRAM stacked package integrated with a logic die[6,7,8], are not fabricated by thermal compression bonding. They are fabricated using the wafer-to-wafer (W2W) DBI bonding technology.

Cu-Cu TCB has a long bonding cycle because solid state Cu diffusion is slow. An attempt to increase bonding throughput has been reported by using a patterned glue layer to hold the die in place during pick and placement at lower temperature, followed by a high temperature and pressure process to collectively form Cu-Cu interconnect (Cu/polymer hybrid TCB)[9]. The glue layer does not compensate for the Cu pillar height variation. In addition, it can restrict pitch scaling.

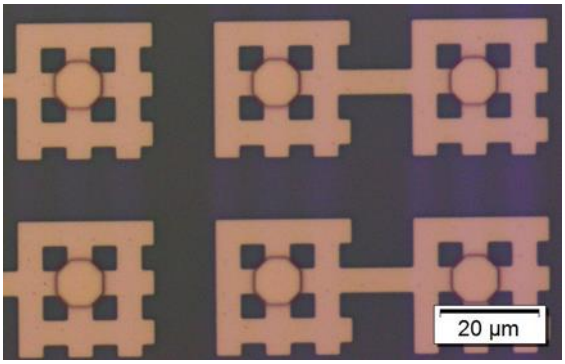
DBI Ultra, a die to wafer low temperature hybrid bonding process[10,11,12,13], has distinctive advantages over Cu-Cu TCB. First, the optimized chemical mechanical polishing (CMP) process offers very precise control of the Cu pad height variation across the entire bonding surface, making it possible to form Cu-Cu bonding at low anneal temperatures. Second, this technology bonds metal pads slightly recessed from the surrounding inorganic dielectric (oxide for this study) surface. The bonding is a two-step process. In the first step the ultra-smooth dielectric surface bonds spontaneously upon contact at room temperature. The bonding strength at room temperature is sufficient to hold the parts together. There is no need for external pressure for the second step, which is a batch anneal process (150–300ºC). The direct Cu-to-Cu connection is established during the heated anneal. Since oxide bonding takes place at room temperature, Cu oxidation during bonding is not a concern. The bonded dielectric layer surrounding the Cu interconnect encapsulates the joints from the environment in the annealing oven; thus minimizing Cu oxidation during the anneal process. The bonded oxide surface also hermetically seals the Cu interconnect during device operation.

In our previous publications, we have demonstrated superior Cu recess control through a robust CMP process. We have also demonstrated a high through-put, high-volume production-ready process with an interconnect pitch as low as 10 µm. Previously, we have reported electrical test yields up to 92% of the die on wafer have 100% of the daisy chain covering a 50mm^2 area fully connected. We have also conducted reliability testing in environmental stress tests including temperature cycling, high temperature storage and autoclave testing. We doubled the test duration required by the JEDEC specification to demonstrate the superior performance. After the tests, all parts showed no increase in resistivity, no crack initiation or defect growth. The parts shown in the previously published work were annealed at 300ºC for 1 hour, which is suitable for many applications. This paper presents the continuation of the DBI Ultra D2W bonding development effort for low temperature applications such as packaging of dynamic random access memory (DRAM) die.

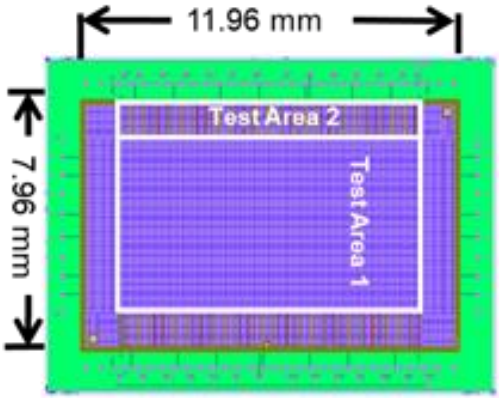
TEST DIE DESIGN AND FABRICATION

The test die design is shown in Figure 1a. The objective is to demonstrate a very high bonding yield of the technology. We choose a daisy chain design with a 10 µm diameter pad on 40 µm pitch in order to conduct bonding with existing high volume flip chip bonders. The alignment accuracy of such bonders ranges from 5 to 10 µm. We optimized the bonder alignment to achieve <5 µm alignment accuracy in order to bond the die with 10 µm circular Cu pads. The die size is 7.96 mm x 11.96 mm. It is a very similar size to a typical DRAM HBM

die. Its fabrication includes two Cu damascene processes for the two metal layers. The image shown in Figure 1 includes a bonding layer, which consists of circular 10 µm diameter Cu bond pads embedded in silicon dioxide, and a Cu trace layer in the shape of a grid for daisy chain connection. The pattern on the die forms half of a daisy chain structure. The other half of the daisy chain structure is on the mating host wafer surface. The die size on the host wafer is enlarged in both the X and Y directions to enable probing of the test pads for a resistance measurement. The main daisy chain in test area 1 shown in Figure 1b has 31356 links with no redundancy and covers 50mm^2 of bonding area. The daisy chain continuity results reported in this paper are from test area 1.



(a)



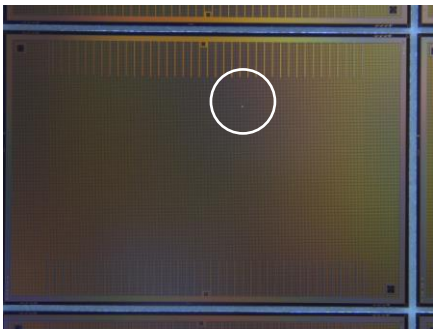
(b)

Figure 1: (a) Optical image of circular Cu bond pads and grid RDL layers in the test die design. (b) Illustration of the bonded D2W daisy chain pair. The purple area is the die on the top, the green border is the over-sized area with probe pads on the host wafer.

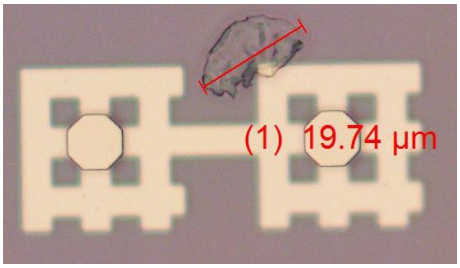
WAFER AND DIE PREPARATION FOR BONDING

Wafers are diced either mechanically or with laser stealth dicing on tape frame and cleaned with our standard process. To minimize contamination from the die preparation steps, the entire clean and bond preparation process is carried out with the die on the dicing tape. Processing die on tape is well suited for a low-cost high-volume manufacturing application.

An ultra-clean die surface is required for void-free bonding and this is the major difference between a solder interconnect and DBI Ultra bonding. For example, the residue shown in Figure 2(a) and (b) is thin and does not cover any bonding pad. For a solder interconnect, it will be encapsulated by the underfill and will not cause any electrical failure. However, for DBI Ultra bonding, since there is no buffer zone at the bonding interface to accommodate the residue, it must be removed to prevent bonding voids that can lead to electrical failure. For the material system we are currently using, we have developed chemical cleaning solutions to remove the residue. As shown in Figure 2(c), the residue was completely removed after cleaning with chemistry B. After the wet clean, the die is treated in plasma prior to bonding.



(a)



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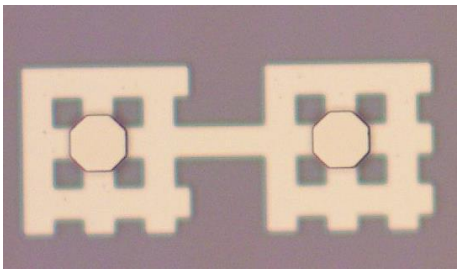


(c)

Figure 2: Effect of different chemistries to remove surface contamination. (a) A low magnification picture of a die on a dicing tape frame after it was cleaned with chemistry A. The small white dot in the circle is a contaminant; (b) Optical image of the contaminant in (a) at higher magnification; (c) The contaminant shown in (b) was completed removed after cleaning with chemistry B.

The preparation of the host wafer for bonding is much simpler because the CMP process to condition the surface to meet the oxide roughness and Cu recess specification for hybrid bonding is very clean. The wafer only requires a rinse in de-ionized (DI) water and a plasma treatment prior to bonding.

BONDING AND ANNEALING PROCESS

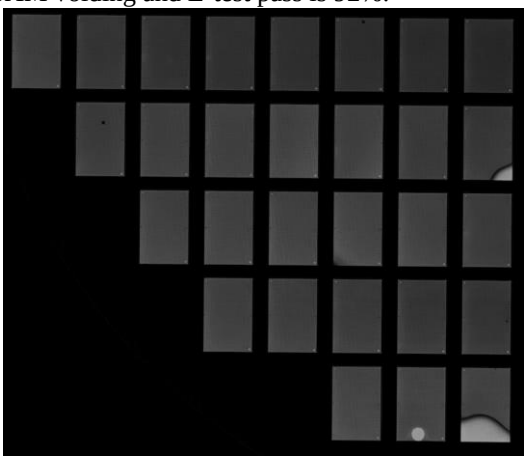
We used a Datacon Evo 2200 flip chip bonder to pick and place die directly from a dicing frame to a host wafer. The process is similar to a standard flip chip pick-and-place process without flux dipping. The bonding is a two-step process: Spontaneous dielectric bonding at die placement, followed by a batch anneal in a convection oven. Dielectric bonding takes place at an ambient environment (~25^{o}C). There is no need for any heating at all – no heated stage or bonding head or inert environment. We generally achieved >90% void free bonding yield in a 1K cleaning room prototype laboratory. Higher yield is expected in a high volume production environment.

Once the entire lot is bonded, the host wafer is put through a heated anneal process in a convection oven. If there is no exposed metal structure, the anneal can be done in air since the DBI Cu pads are fully sealed by the bonded oxide and there is no Cu oxidation concern during anneal. In order to minimize the thermal budget and more accurately represent time at temperature, we adopted a hot-in/ hot-out anneal process. We place the wafer inside the convection oven after the oven is stabilized at 200^{o}C and take it out after 60 minutes in the oven.

To assess correlation of Cu recess and annealing temperature requirement, samples with varying Cu recess were produced, bonded and tested after annealing.

RESULTS

Figure 3 shows results from a test piece with medium Cu recess. Figure 3a is an image from confocal scanning acoustic microscopy (CSAM) focused at the bond interface. Figure 3b shows the corresponding electrical continuity test results in the large test area 1 shown in Figure 1b. The test area has 31,356 daisy chain links with no redundancy and covers a bonded area of 50 mm^2. The CSAM image showed 3 die with bonding voids affecting the test area. The electrical continuity tests show an open circuit for the same 3 die with voids. In addition, two die which do not show visible voids also showed electrical open. For this build, the correlation between C-SAM voiding and E-test pass is 92%.



(a)

Pass	Pass	Fail	Pass	Pass	Pass	Pass	Pass
	Pass	Pass	Pass	Fail	Pass	Pass	Fail
		Pass	Pass	Pass	Pass	Pass	Pass
			Pass	Pass	Pass	Pass	Pass
					Pass	Fail	Fail

(b)

Figure 3: (a) CSAM image of sample piece showing 3 die with bonding voids affecting test area 1. (b) Corresponding electrical continuity results for the daisy chain test area 1 with 31356 links. Green indicates electrical continuity and red indicates electrical open.

The two die which show no visible void did have electrical opens explained by deeper than average Cu recess. The DBI process depends on Cu expansion due to differential CTE between Cu and the surrounding

oxide to bridge the room temperature recess gap and simultaneous Cu-Cu inter-diffusion. Therefore having shallow and uniform Cu recess for all Cu interconnect is critical for high assembly yield.

As we have shown in prior publications, we have developed a robust CMP process to achieve precise control of the Cu recess for various pad sizes. With the current design and shallow Cu recess, we have 100% correlation between the CSAM voiding and daisy chain electrical open. Table 1 summarizes the evaluation results from multiple builds.

Table 1: Correlation between CSAM voiding and E-test pass after 200ºC/1 hour anneal.

Build	Cu recess	Anneal Temperature (C)	# Die Pass E-test/# Die No void	% E-test pass
1	Medium	200	24/26	92
2	Shallow	200	20/20	100
3	Shallow	200	19/19	100
3	Shallow	200	13/13	100
3	Shallow	200	15/15	100

We cross-sectioned several E-test passing samples to examine the quality of Cu-to-Cu bond and we found a high quality metallurgical bond at the interface. One example is shown in Figure 4.

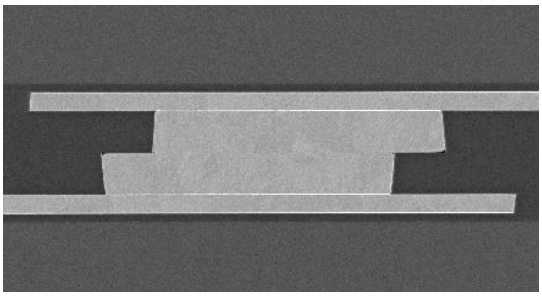


Figure 4: SEM cross-section of a bonded Cu-Cu joint after 200ºC/ 1 hour anneal.

DISCUSSION

The basic requirement of die packaging/stacking is to have all electrical joints connected permanently without bridging. Due to manufacturing process limitations for a TCB µbump process, there are inherent height variations of several microns between the bumps to be connected on both sides. In addition, parts can warp during the thermal process to connect the pads on both sides. Such height variation is overcome by the melting and re-solidification of the solder since the liquid solder can wet the two surfaces to be joined and be stretched or compressed to compensate for the height differences and maintain its shape when it re-solidifies. However, the physical deformation allowed for solder depends on its volume. With the progressive pitch reduction, the compression of liquid solder causes solder bridging and shorted joints below 60 µm pitch. The problem was partially alleviated by the TCB µbump technology, which reduces solder volume by using a Cu pillar under the solder cap. However, limiting the volume of solder creates a challenge to bridge the +/- 2 µm gaps mating µbumps during the melting and re-solidification process. As shown in an analysis by Gao[14], at 45 µm interconnect pitch, the process can compensate for approximately 7 µm of height difference. However, at a 20 µm interconnect pitch, the available solder can only compensate for approximately 1 µm height differences. Since the inherent solder bump height variation from the electroplating process is at least several microns, TCB µbump solder connections with a high volume manufacturing process at 20 µm pitch is fundamentally unattainable. The packaging industry appears to be stuck around a pitch of 40 µm, thereby supporting this thesis. The consensus within the industry is that further pitch scaling requires solid Cu-to-Cu bonding.

DBI Ultra is the most promising technology among the different Cu-to-Cu bonding approaches currently in development due to three key characteristics of the process: 1) nanometer scale Cu pad height variance through the CMP process; 2) hermetical seal of the Cu pads prior to heated anneal which prevents Cu oxidation during annealing and through the entire service life of the part; and 3) comparable bonding throughput to mass reflow flip chip technology.

For all solid Cu-to-Cu joining technologies, no metal melting is available to compensate for height variations across different pads, it is therefore critical to have pads with very low variance and small gaps that can be bridged during the heated bonding or annealing process.

Figure 5 illustrates the gap between opposing Cu pads at a bonding interface for DBI Ultra. Since the reference surface is defined by the oxide-to-oxide bonded interface, the gap between Cu pads are the sum of Cu recess on the both sides. With the robust CMP processes we have developed at Xperi, we have achieved shallow and uniform Cu recess[13]. Compared to the solder joint height variations of several microns, the Cu recess variation

from the DBI CMP process is only a few nm, which represents 3 orders of magnitude improvement. The gap is bridged by expansion of the Cu pads during the final anneal process accompanied by simultaneous Cu diffusion across the interface to form permanent Cu-to-Cu bonding.

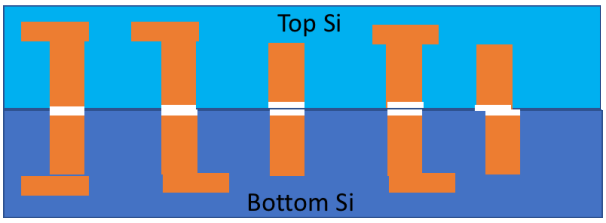
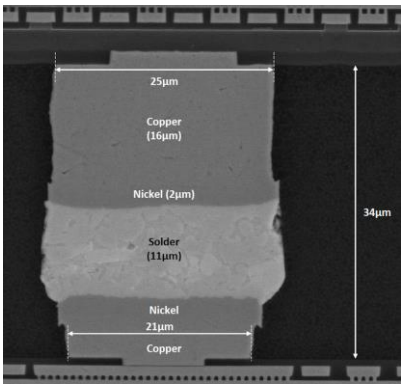


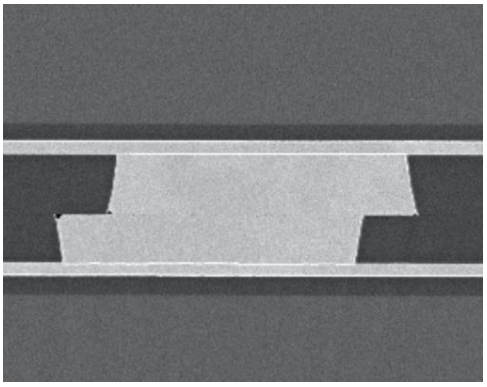
Figure 5: Illustration of Cu pad height variation at a DBI Ultra bonding interface

Compared to the TCB µbump technology, DBI Ultra provides a pathway to generations of further pitch scaling, while offering additional technical advantages: Pitch scaling, total package height reduction, superior interconnect reliability and hermetic package performance are demonstrated advantages. W2W DBI bonding at 1.6 µm pitch has been demonstrated. Currently the pitch scaling limit for DBI Ultra is the alignment accuracy of the bonder. We have demonstrated 10 µm pitch interconnect using a bonder with +/- 2 µm alignment accuracy[11]. Further pitch reduction can be enabled by improving the bonder alignment accuracy.

The second advantage is package height reduction. Figure 6 shows a cross-sectional comparison of TCB and DBI Ultra interconnects. The stand-off height of a TCB µbump is 20-40 µm (Figure 6a); however, with DBI Ultra, the height is reduced to zero, as shown in Figure 6b.



(a)



(b)

Figure 6: Comparison of cross-sections of (a) TCB µbump (Courtesy: System Plus Engineering); (b) DBI Ultra Cu-Cu bonding.

The third advantage is improvement in reliability. The very large CTE mismatch between the underfill and the Si is a large driving force for crack initiation and growth in temperature cycling. Additionally, intermetallic formation between solder and the Cu is problematic, leading to additional void growth under bias. Both problems are eliminated with the DBI Ultra bonding. Since no underfill is present, there is no driving force for crack initiation. Elimination of solder removes intermetallic growth at the interface, leading to stable joints and higher current carrying capability.

The hermetic bonded oxide formed at ambient with the DBI Ultra bonding technology is beneficial. It keeps the Cu pads free from oxygen during the anneal process, enabling low temperature annealing to form the Cu-Cu bonding. After the part is annealed, it protects the Cu interconnect from further oxidation in the field service environment. In fact, the extended exposure to higher temperature provides additional annealing for the Cu joints, improving the joint reliability.

A competing approach to solid Cu-to-Cu bonding is Cu-Cu TCB, which bonds Cu pillars protruded above the Si surface at high temperature and with high pressure. Figure 7 illustrates the fundamental challenge with Cu pillar height variation this technology faces. These pillars are formed by electroplating in holes defined by a patterned resist layer. Height variation > 1µm is common. During the bonding process, the bond interface is defined by the highest pillar.

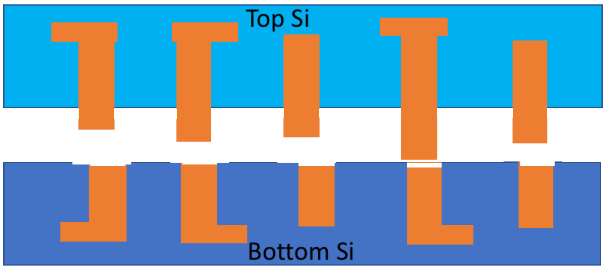


Figure 7: Illustration of Cu pillar height variation at a TCB interface

Since there is no metal melting to compensate for the height differences, the process relies on deformation of Cu under higher temperature (commonly above 350°C) and high pressure (commonly >250 MPa) for a duration of at least 15 minutes. One deficiency with this process is that the high temperature causes rapid Cu oxidation. At ambient condition, a clean Cu surface forms a layer of oxide which is approximately 2-3 nm thick[15]. However, at 300°C, 1 minute exposure results in a Cu oxide thickness of 300 nm and 30 minutes exposure resulted in 450nm thick oxide layers[16]. As a result, bonding needs to take place in vacuum or special gas environment (inert or reducing), which is not attractive for high volume assembly. Finally, the high pressure adds risk for thin die fracture due to non-uniform distribution of stress at high and low posts.

Experimental attempts to improve the Cu pillar height variation by diamond bit fly cutting has been reported[3]. The study reported the Cu pillar height variation across a 200 mm wafer was 600 nm after planarization. This number is two orders of magnitude higher than the Cu height variation from a CMP process. The smallest Cu pad diameter reportedly planarized by this method is 20 µm. Considering the high impact force on the Cu pillar during the fly cutting process, it is questionable whether smaller size pillars can survive the cutting process without breaking.

Various attempts have been made to increase bonder throughput of the Cu-Cu TCB process. One example is Cu/ polymer hybrid TCB[9]. The process applies a patterned tacky glue layer on the wafer side. The die with protruded Cu pillar is picked and placed with the glue holding it in place. Once the entire wafer is populated, a second stage bonding process deforms and flows the polymer layer at high temperature and pressure to allow the Cu pillar on the die to contact the Cu pads on the wafer and collectively form Cu-Cu bond. As illustrated in Figure 8, the glue layer has no effect in compensating for the Cu height variation. In addition, the process requires deformation of the tacky glue layer. Sufficient spacing between Cu pillars/pads and the glue is required to prevent the glue from getting between the Cu pads on the wafer and the Cu pillars on the die to cause open failure. This requirement can limit pitch scaling ability. The paper gives no information on the interconnect pitch for the study.

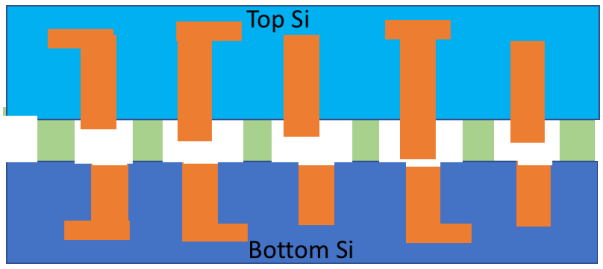


Figure 8: Illustration of Cu pad height variation at a Cu/ polymer hybrid bonding interface with a layer of patterned adhesive on one side prior to die placement.

For the Cu-Cu TCB process, after the Cu-Cu bonding is complete, the gap between the two die needs to be filled to prevent Cu oxidation in the field service. Filling the small gap between the two bonded Si surfaces is very challenging. No good solution has been reported in the literature.

Table 2 provides process comparisons between DBI Ultra and a variety of Cu-Cu TCB processes. DBI Ultra is superior and minimizes Cu height variation, bond and anneal temperatures and pressure and increases pitch scaling, and bonding process throughput while preventing Cu oxidation in field service.

As we mentioned in the introduction, various approaches to reduce Cu-Cu bonding temperature have been studied and reported. However, they all suffer the same fundamental problem of high Cu height variation for the -Cu TCB process.

Table 2: Process comparison for DBI Ultra and several variants of Cu-Cu TCB.

	DBI Ulta	Cu-Cu TCB	Cu-CU TCB with fly cutting	Cu/ polymer hybrid TCB with fly cutting
Cu Height variaiton	< 3nm over 12" wafer	> 1um over 8" wafer	~600 nm over 8" wafer	~600 nm over 8" wafer
Finest pitch demonstated	<1 um (W2W), 10um (D2W)	10um	40um	No data
Pitch limiting factor	Bonder alignment accuracy limit	Cu pillar plating process limit	Cu pillar breakage during fly cutting	Cu pillar breakage during fly cutting
Bonding temp	room	>300C	>300C	>300C
Bonding pressure	None	>250 MPa	>250 MPa	>250MPa
Bonding duration	< 1s	15-60 min	15-60 min	No data
Anneal temp	150C-300C			
Vaccum or inert environment	No	Yes	Yes	Yes
Cu oxidation in field service	No	Yes	Yes	No data

SUMMARY

The DBI Ultra D2W low temperature direct bond interconnect technology holds the promise for many generations of interconnect pitch scaling below 40 µm. We have demonstrated bonding at 10 µm interconnect pitch in an earlier publication. In this paper, we have demonstrated that the technology is suitable for applications with a maximum 200ºC anneal temperature restriction. We have assembled a daisy chain test die with a test area covering 31356 links and 50mm^2 surface area. We achieved good electrical test yield after 1 hour of anneal at only 200ºC. One key enabling factor is the robust CMP process we developed to achieve very shallow and uniform Cu recess across an entire 12" wafer. SEM images of the cross section showed a solid Cu-Cu metallurgical connection across the bonding interface.

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