RECENT DEVELOPMENTS IN FINE PITCH WAFER-TO-WAFER HYBRID BONDING WITH COPPER INTERCONNECT

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ABSTRACT

3D architectures are increasingly making their way into commercial products such as image sensors and 3D memory. While hybrid bonding exists today in wafer-to-wafer (W2W) format in high volume manufacturing, the proliferation of this technology continues to accelerate. A wide range of new products may be considered by leveraging the ability to connect circuit elements fabricated with two different process technologies. For example, some NAND architectures are monolithic 3D devise which are formed using processes with divergent thermal requirements such as the high temperature memory technology and the lower temperature logic. This monolithic approach is the standard today but leads to a final product that is a compromise of the thermal budget constraints. Alternatively, disaggregation of the memory components and the logic components onto separate wafers would allow each technology to be optimized independently with potentially different thermal budgets. Using Cu based hybrid bonding, a fine pitch Cu interconnect may be used to then join the two wafers at temperatures well below 400ºC while achieving superior I/O performance within a smaller footprint [1].

Direct Bond Interconnect (DBI®) technology, is a low temperature hybrid bonding process that forms a dielectric-to-dielectric bond at room temperature and a metal-to-metal bond at the appropriately designed temperature. It is the key enabling technology for advanced products because of its unique ability to bond wafers at low temperature and to successfully bond pads ranging from 1.9 μm to 15 μm diameter. The corresponding pitches range from 3.8 μm to 40 um. Generally, a low temperature anneal process of 150 – 400ºC can be achieved. The all-Cu interconnect across the bond interface provides good electrical performance and enhanced reliability. [2]

This paper presents bonding and electrical yield results with a test vehicle design that demonstrates high-density, fine pitch bonding with high-yield. The test vehicle consists of daisy chain test patterns with 4 μm bonding pitch with 115k links and covers a bond area of 3.61 mm^2. The process flow enables high throughput processing with room temperature bonding and post-bond batch anneal. The process shows minimum electrical yield greater than 98% across all wafers. Longer chains of 500k links with a 3 μm diameter pad with a 10 μm pitch show similar yields. Temperature cycling and autoclave tests of the 3 μm diameter pad test structures showed a robust Cu/Cu interconnection and superior reliability performance.

INTRODUCTION

The 3D interconnect market is steadily growing as the requirements for high I/O density and enhanced performance increase. Meanwhile, there is ever present pressure to lower packaging costs. Hybrid bonding (such as DBI®) is an attractive technology to meet the needs of wide I/O bonding interfaces due to the scalability to fine pitch. Low-temperature hybrid bonding in a wafer-to-wafer format has been used for several years in volume production for back-side illuminated CMOS image sensors [3]. Similarly, the advantages of hybrid bonding combined with disaggregation can be realized in true heterogeneous integration between memory and logic or III-V and CMOS. Using the hybrid bonding architecture, one manufacturer recently released a NAND flash with the highest density among peer-group products disaggregation of memory from logic. [4,5]

Hybrid bonding connects the planar damascene surface of the integrated circuit without the need for any intermediate materials like solder or adhesives. Instead an instantaneous chemical bond is formed between the mating dielectrics on each wafer. As the temperature increases in the batch anneal process, the bond strength between the dielectrics increases and the expansion of the mating Cu pads closes the small gap between them. This allows Cu-Cu diffusion to take place securing an electrical interconnect across the bond interface. Batch processing also widens accessible time and temperature ranges to lower temperatures and longer times if needed for thermal budget restrictions on certain materials. Moreover, this hybrid bonding technology has no equivalent wafer bonding alternative, because the amount of force required for a wafer-to-wafer bonding environment with Cu/Cu thermal compression bonding would be excessively large for high I/O Cu interconnects.

Advantage of Fine Pitch Hybrid Bonding

The primary advantage of fine pitch layout is the high interconnect density. As the interconnect pitch requirement drops to 4 μm and below, hybrid bonding becomes an attractive solution, due to the pitch scaling capability, room temperature bonding and low temperature final anneals. True heterogeneous integration is made possible with the low temperature final anneal with the hybrid bonding technology.

3D-NAND Flash devices are known to suffer performance related issues and inefficient use of silicon area due to process compromises from integrating logic and memory onto one wafer. It is important to use high conductivity polysilicon which occurs as the deposition temperature increases toward 600ºC [6]. However, the control logic in NAND has higher voltage and lower speed

performance in the integrated product compared to advanced CMOS logic nodes where the temperature is kept between 250ºC to 350ºC. In monolithic 3D structures, the logic shares the same thermal processing steps as the memory elements which may reach temperatures in excess of 500ºC [6]. Recent efforts to eliminate this constraint use wafer-to-wafer hybrid bonding; whereby logic and memory portions of the flash NAND are processed on separate wafers and bonded at control logic-compatible temperatures [5]. Since the control logic and memory element circuits have roughly similar areas, a wafer-to-wafer process flow offers a substantial x-y footprint space savings.

The objective of this work is to show the readiness of hybrid bonding for fine pitch wafer-to-wafer application. We demonstrate high electrical yield and reliability performance of Cu interconnects at relatively low anneal temperatures for a pitch of 3.9 um and 10 um with hybrid bonding technology.

Wafer-to-Wafer Hybrid bonding Process

One version of hybrid bonding utilizes a single damascene layer which may be added to any incoming wafer. The layer definition should consider the thermal budget and planarization requirements. Sometimes the single damascene layer is integrated within the last metal layer of the device for cost savings. The damascene layer consists of metal bond pads surrounded by a dielectric. The hybrid bonding pads for this work are copper and the dielectric surfaces are PECVD SiO_2. The dielectric layer serves to isolate the pads and provide the initial bonding surface when the wafers are brought in contact. Each wafer has a hybrid bonding layer with pads arranged to align with the mating surface.

One key enabling aspect of hybrid bonding technology is the ability to produce an engineered flat dielectric bonding surface across the entire wafer. The bonding pad layout is an important consideration since it influences the CMP process window for creating the surface. We have developed a robust process which allows integration with pads ranging from 1 um to 15 μm in diameter.

The overall process flow utilized for this work is shown as a schematic in Figure 1. Starting with a wafer that has a flat surface, the hybrid bonding layer is formed by a damascene process flow. The wafer is then polished using CMP. Anything that interferes with the flatness, roughness, or surface state is removed. A thorough post-polish clean ensures the surface is particle and contaminant-free.

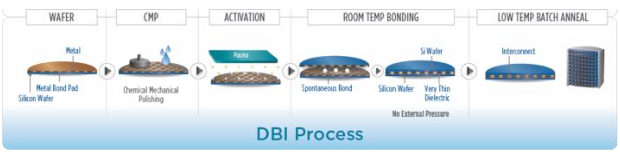

Figure 1: Overview of the wafer-to-wafer hybrid bonding process flow.

After the surface has been prepared and cleaned, it is chemically activated through a plasma activation process. This step creates active sites that form chemical bonds between the two dielectric surfaces. The bond strength comes from the surface modification of the dielectric. The interatomic bond strength between dielectrics holds the wafers together. While the plasma process activates the dielectric, it does not interfere with the ability of the metal surface to fuse later during the anneal step.

The wafers are aligned and brought into contact to form the initial dielectric-to-dielectric bond, (refer to Figure 2 for the hybrid bond formation schematic). This holds the two wafers together with enough force that the bonded pair can be freely handled while maintaining alignment, acting much like a built-in thermal compression bonding fixture. The key to fine feature bonding is controlling fabrication of both wafer surfaces to minimize runout and contacting of the surface such that only one bond-front forms and propagates across the wafers. The dielectric bond forms at room temperature eliminating issues with differential thermal management during bonding.

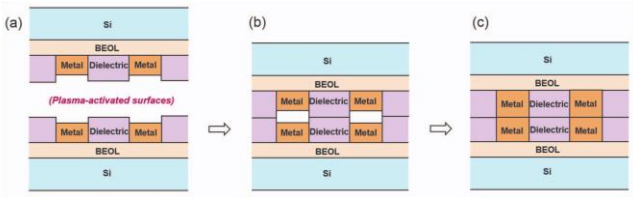

Figure 2: Hybrid bond formation schematic- a) hybrid bonding surfaces prior to bonding, b) initial room temperature state after aligned bonding and initial dielectric-to-dielectric, and c) completion of copper-to-copper bond after annealing [7].

The annealing process forms the hybrid bond through a two-step and largely simultaneous process. Heating accelerates chemical bond formation further strengthening the dielectric interface and drives the copper pads to a metallurgical bond. As the temperature increases, the copper surface energy provides a driving force and diffusion continues to join the pads forming a strong metallurgical bond. Another advantage of the bonded dielectric layer is that it protects the metal surface from oxidization during the anneal process which may occur in ambient conditions. The annealing process window in this study ranges from 250°C to 350°C; however, successful hybrid bonding final anneal temperatures can range between 150°C to 400°C.

The hybrid bonding process flow is versatile and works for a wide variety of metal layouts with bond pad dimensions ranging from 1.9 μm to 15 μm. The 1.9 μm pad is fine enough to ensure no circuit design limitation while the 15 μm pad is large enough to ensure adequate pad overlay on all modern bonding equipment. The hybrid bonding process has been demonstrated on bond pad pitches of 3.8 μm to 40 μm. The main limitation in demonstrating finer pitch has been access to bonders with reliable alignment capabilities. One key advantage of the technology is that the same process may be applied to a broad range of interconnect pitches and bond pad diameters.

EXPERIMENTAL DESCRIPTION

The purpose of this work is to show electrical yield and reliability of fine pitch hybrid bonding at low temperatures in

a wafer-to-wafer format. Two test wafer designs are evaluated. One design has a daisy chain array of 1.9 µm diameter bond pads on a 3.8 µm pitch (referred to as 1.9x3.8) daisy chains. The second test wafer design has an array of daisy chains with a 3 µm diameter bond pad on a 10 µm pitch (referred to as 3x10). The purpose of the 1.9x3.8 test vehicle is to test the electrical yield as a function of anneal conditions on good Cu metallurgical bonding. Reliability tests were performed on the 3x10 test vehicle.

Test Vehicles

The wafer layouts are both designed to be self-bonding so that both halves of the daisy chain are placed on a single wafer in a staggered arrangement. When one wafer is flipped over onto the other wafer, all of the devices create functional daisy chains. The 1.9x3.8 daisy chain has 115k links and covers an area of 3.61 mm^2. Figure 3a shows a close up schematic of a daisy chain with the rotation axis shown in green to show the self-bonding concept. The left pattern folds over the right pattern on the symmetry axis to complete a serpentine daisy chain. Figure 3b shows the overall staggered device layout. The 3x10 daisy chain has longer chains of 500k links and a die size of 50.4 mm^2. Figure 4 shows a close up of the 3x10 layout for the daisy chain in the aligned state. The hybrid bonding layer thickness for both devices in this study is approximately 1.0 µm, and the underlying inter-connect layer thickness is 0.20 µm.

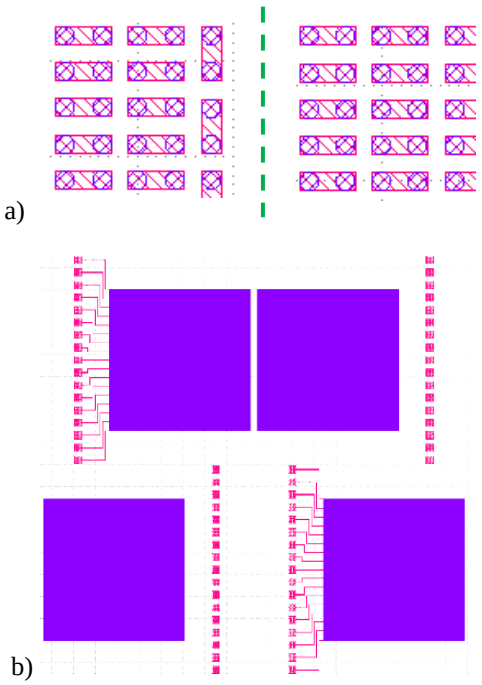

Figure 3: a) A magnified image self-bonding daisy chain of the left and right side of the die for the 1.9 µm hybrid bond pad on a 3.8 µm pad pitch with vertical self-bonding, the rotation axis for self-bonding symmetry is in **GREEN** in an unbonded state, b) overview of self-bonding hybrid bonding daisy-chain layout, alternating locations on the left bond to locations on the right to form completed circuits. **RED** is the underlying interconnect layer, and the **PURPLE** is the hybrid bonding layer.

Process Flow Specifics

The prototype test wafers are 200 mm wafers fabricated at L'Foundry. The hybrid bonding surfaces were polished, prepared, and bonded by Xperi's prototyping wafer facility. Aligned bonding at room temperature in an air ambient was performed on a modified Laurier CBD50 bonder capable of wafer-to-wafer bonding with less than 1.0 µm alignment. Annealing was performed in a batch annealing oven. Six 1.9x3.8 wafers pairs were used for the thermal processing work, and one 3x10 wafer was used for the reliability work. Post bond processing includes grinding the top wafer to 20 µm, exposing the probe pads with a dry silicon etch and a dry oxide etch. The two-point resistance test system is a manually operated Rucker and Kolls probe station using a Hewlett Packard 3478A multi-meter with 150 mm travel. Wafers were annealed at various temperatures and the electrical resistivity measurements were made after a single anneal.

RESULTS

A robust baseline process with a known high yield anneal condition as utilized in these studies to examine the sources of chain resistance variation within the wafer pairs. Then reliability studies are presented.

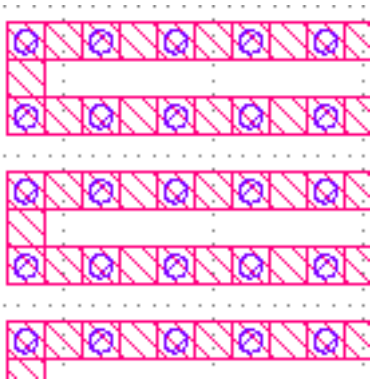

Figure 4: Schematic of daisy-chain layout for 3 µm hybrid bond pad diameter on a 10 µm pad pitch in an aligned state.

Bonding Alignment and Yield Summary

Figure 5 shows optical images of the device wafers after the final CMP for the 3x10 daisy chains. Both halves of the self-bonding daisy chain structure are shown in Figure 5a and 5b. The large pads are used to measure the full length of the chain.

Figure 6 is a cross section of the 1.9x3.8 daisy chain used in this experiment, showing complete bonding of both the dielectric-to-dielectric interface and the copper-to-copper connections. The image shows void-free bond interface with a good Cu-Cu metallurgical bonds. Based on the measured thicknesses of the cross sections, the theoretical chain resistance associated with the copper line resistance is 19073Ω. Wafer-to-wafer alignment was measured at two points at approximately -80 mm and +80 mm near the horizontal axis of the wafer, (see Figure 7 for an example). Table 1 lists processing summary and electrical results for all wafer pairs of the 1.9x3.8 material. The yield is calculated as all daisy chains with chain resistance within 3 sigma of the minimum measured resistance.

Bond misalignment determined by x and y verniers ranges from 0.57 to 1.7 µm, (Figure 7). Wafer pair 6 has a 1.7 µm misalignment with an associated yield loss of ~60% due to the lack of contact area. However, the mean misalignment for the remaining 5 wafer pairs was +/-0.75 µm, with a standard deviation of 0.18 µm. For these cases <0.95 um misalignment, no significant correlation between bond alignment and yield or mean resistance was observed.

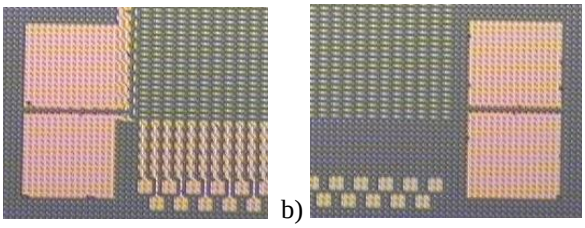

Figure 5: Optical images of array edge and probe pads for 3x10 daisy chain. The circles are hybrid bond pads with a pitch of 10 µm in between them.

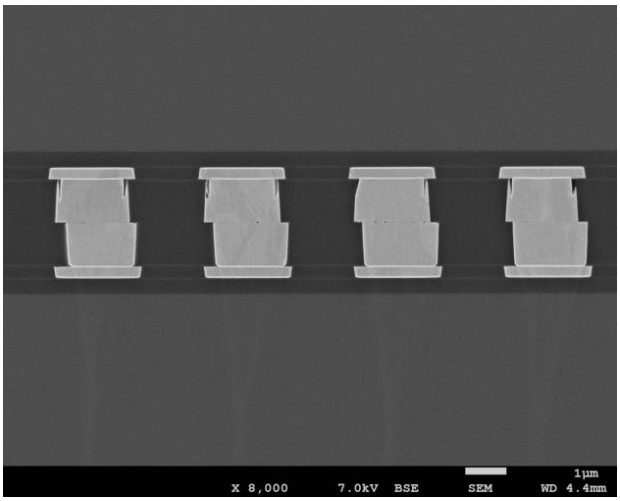

Figure 6: Scanning electron micrograph of hybrid bond cross section of wafer pair 3 (1.9x3.8 daisy chain), annealed at 350°C for 0.5 hr.

Electrical resistance results are shown as a function of for final anneal conditions in Table 1 For each wafer, 43 daisy chains are measured. Chain resistance ranges from 19500 to 23000 Ω (0.17 to 0.20 Ω/link), with bond misalignment from 0.57 to 0.95 µm. There is no statistical correlation between translational alignment and electrical resistance or yield for a simple x-y translation misalignment below 0.95 µm. Wafer pair 6 shows a substantially lower yield 43% which is attributed to a 1.7 µm translational misalignment so the hybrid bond contact area is less than 10%. Additionally, pair 6 had the highest rotational alignment error and the highest excess chain resistance, 5800 Ω, for all wafer pairs. The yield loss in pair 6 was associated with die near the wafer edge, so there may be some rotational alignment contribution as well. For the entire dataset, there is a correlation between rotational misalignment and higher resistance, as shown in Figure 8, with a R^2 of 0.70. The plot implies that the wafer-to-wafer repeatability is controlled by rotational misalignment.

The chain resistance yield is high for a thermal budget of 300°C for 0.5 hr or more (98.7% to 100%). The lowest thermal budget of 300°C for 0.5 hr, yielded 100% indicated sufficient thermal energy was used in the subsequent samples.

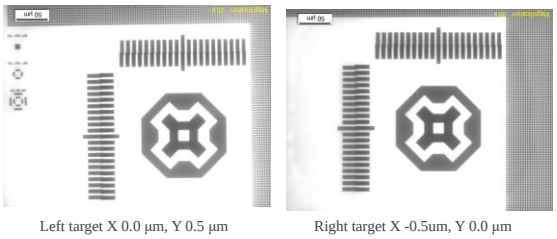

Figure 7: Example infrared images of alignment verniers for wafer bond alignment measurement on the 1.9x3.8 test vehicle.

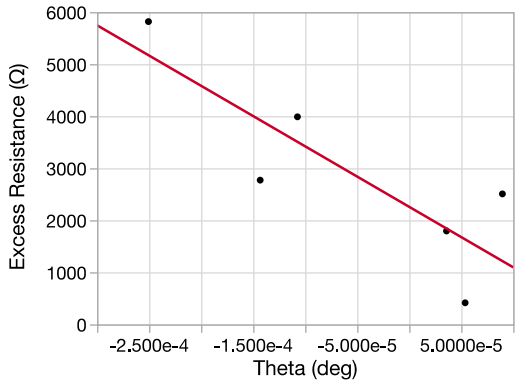

Figure 8: Relation of rotational error to excess chain resistance for the 1.9x3.8 bonded pairs.

Table 1: The bond misalignment, final anneal conditions, and yield of 1.9x3.8 daisy chains is shown for six pairs.

Pair	Maximum Bonding Displacement (µm)	Final Anneal Temperature (°C)	Final Anneal Time (hr)	Final Mean Resistance (Ω)	Final Yield (%)	Excess Resistance (Ω)
1	0.95	300	0.5	20768	100.0	1708
2	0.61	350	2.0	21580	98.7	2552
3	0.57	350	0.5	19487	98.7	414
4	0.71	350	2.0	23061	100.0	3988
5	0.95	350	2.0	21844	98.7	2771
6	1.70	350	2.0	24891	43.3	5818

Chain Resistance Analysis

Electrical performance of wafer pair 1 for the 1.9x3.8 test vehicle is shown in Figure 9, which is typical for the set of wafers, with a mean resistance of 20768 Ω and a standard deviation of 365 Ω (2%). The resistance map in Figure 10 shows a portion of the wafer from the center towards the edge of the wafer along one side. The map shows a center-high resistance, a lower resistance for mid-radius devices, and a slight resistance increase at the wafer edge. The within-wafer resistance non-uniformity is in the same range as the thickness non-uniformity of the underlying interconnect layer (2%), and follows the same trend as a function of radius,

therefore wafer fabrication variation controls within wafer uniformity.

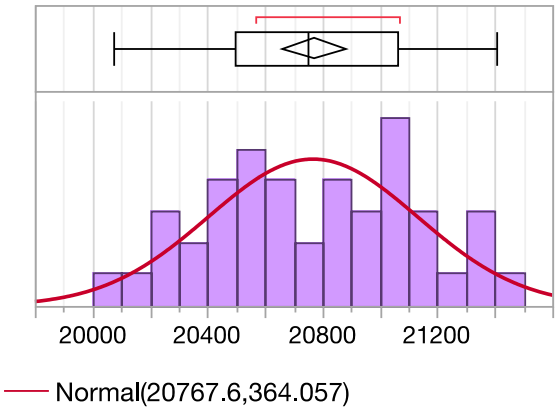

Figure 9: Resistance histogram for the 1.9x3.8 daisy chain (1.9 µm diameter, 3.8 µm pitch) wafer pair 1, 43 die measured.

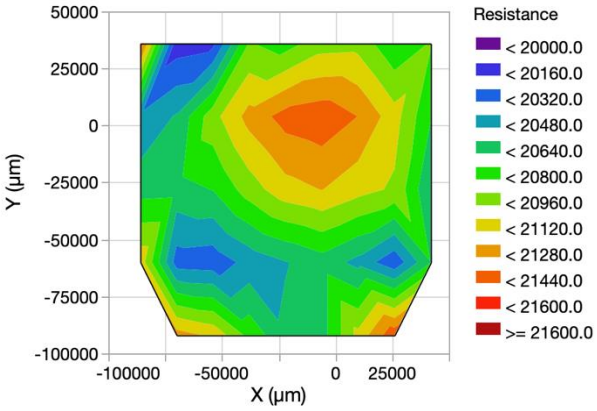

Figure 10: Resistance map for the 1.9x3.8 daisy chain (1.9 µm diameter, 3.8 µm pitch) wafer pair 1. 43 die are measured. The map covers a range of -92 mm to +36 mm in the Y-axis, and -86 mm to +42 mm in the X-axis.

Electrical performance for the 3x10 wafer pair is shown in Figure 11a. It has a mean resistance of 77300 Ω and a standard deviation of 1785 Ω. Electrical yield for this wafer is 98.6%. The standard deviation of the electrical resistance for both test vehicle designs is 2%. The cumulative distribution function in Figure 11a clearly shows the two different distributions and indicates that the variance of the higher resistance distribution is larger than the lower distribution.

The resistance map in Figure 12 shows a slightly center-high resistance with a slight increase again at the wafer edge. Nevertheless, the 3-sigma variation within wafer is only 5350 Ω or 6.9%. The spatial distribution is similar to the 1.9x3.8 test vehicle, except the wafer edge makes up the high end of the distribution, and the center is marginally higher than the mid-radius section. The yield of the wafer was 98.7%. Since the same fabrication process was used for the 1.9x3.8 and 3x10 test vehicles, the underlying interconnect layer thickness variation is likely controlling the resistance change for the 3x10 as well.

Reliability Results

Wafer-level reliability testing looked at the inherent reliability of the hybrid bond using the 3x10 daisy chain. Two tests were performed, temperature cycling (TCT) following the JESD22-A104D Condition B protocol (-55°C to 125°C, 10-14°C/min ramp, 10min dwell, 1000 cycles), and highly-accelerated stress testing (HAST) adhering to the JESD22-A102D Condition D protocol (121°C, 100% relative humidity , 2 atm for 168 hr). The source of parts was a partial wafer with 116 daisy chains for HAST and another partial wafer with 122 parts for TCT. The failure criteria for each test was a 10% resistance increase. All parts passed the complete HAST and 1000 cycle TCT without any failures, (see Table 2 for intermediate and final results).

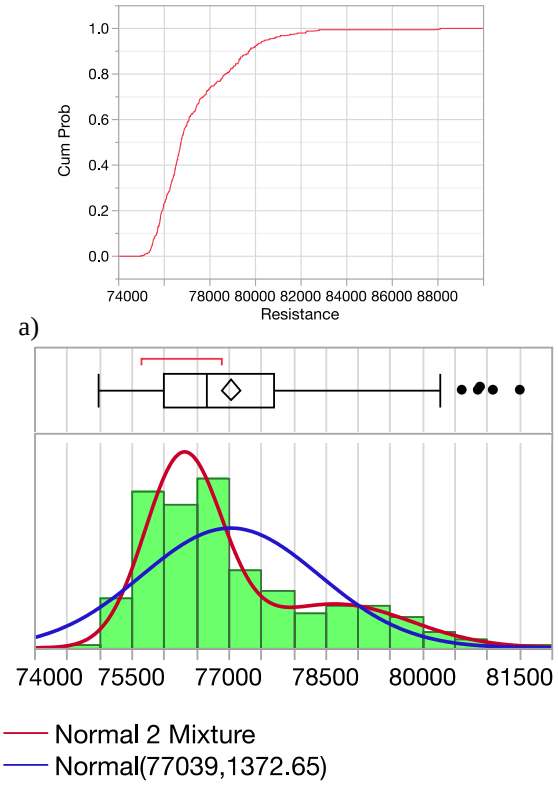

Figure 11: Resistance statistics for 3x10 daisy chains (3 µm diameter, 10 µm pitch). a) cumulative distribution function, b) histogram of the same data. 354 die are measured.

DISCUSSION

The hybrid bonding process is robust and shows excellent process control. One wafer pair was excluded due to poor alignment. The remaining five fine-pitch prototype wafer pairs show high yield, >98.7%. Both within wafer and wafer-to-wafer metal thickness uniformity were found to control the resistance variance across the wafer pair. Lastly, the process demonstrates yield between 87.5-100% for post-bond anneal with a thermal budget as low as 300ºC 0.5 hr.

Reliability results all die passed both thermal cycling and highly accelerated stress tests. This indicates the hybrid bond is robust and agrees with previously published work [8] on die-to-wafer reliability. Therefore, both fine-feature and large feature hybrid bonding test vehicles produce reliable connections between integrated circuits.

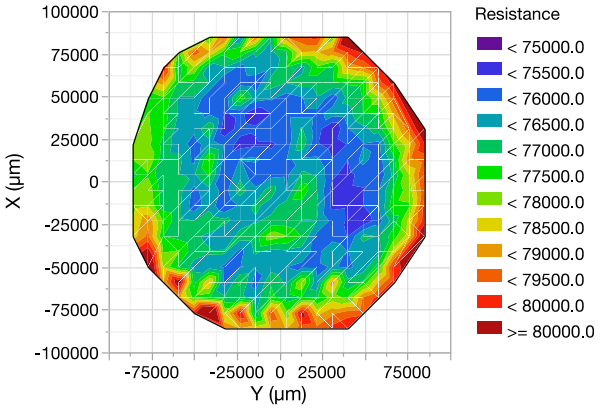

Figure 12: Resistance map of the yielding die for the 3x10 wafer. 354 die measured.

Low temperature hybrid bonding produces high yielding and reliable bonds for fine pitch geometries on multiple device layouts. Yield is high for thermal budgets as low as 300°C for 0.5 hr and shows good repeatability for a prototyping facility with yield >98% on all tested wafer pairs. This shows that the technology is robust and ready to serve as the foundation of advanced fine pitch 3D integrated circuit technologies.

Table 2: Results of reliability tests run.

	Test	Result
1st ½ Wafer	HAST	All parts passed
2nd ½ Wafer	TCT – ~442 cycles	All parts passed
	TCT – 823 cycles	All parts passed
	TCT – 1000 cycles	All parts passed

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