Surface Photovoltage and Contact Potential Difference Imaging of Defects Introduced by Plasma Processing of IC Devices.

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Integrated circuit (IC) manufacturing involves a large number of plasma processes ranging from anisotropic etching, isotropic stripping and cleaning, to plasma enhanced material deposition and implantation. It frequently occurs that undesirable reactions between the partially completed IC devices and plasma environment can lead to detrimental and permanent changes of device properties. Two the most frequently encountered device degradation mechanisms are: 1. unbalanced charge transfer between the wafer and plasma sheath leading to so-called "antennae damage", and 2. "radiation damage" caused by bombardment of the wafer with high energy photons, particles, and ions causing bond breakage, introduction of impurities and formation of intrinsic defects and defect complexes in the Si substrate and in dielectrics. Most of analytical techniques employed for plasma damage detection rely on fabrication of dedicated devices acting as plasma damage sensors[1,2]. They frequently facilitate accurate evaluation of a specific type plasma damage, but at a cost of additional device fabrication, material expenses, and delays needed to fabricate and analyse device sensors. Present work demonstrates application of relatively simple materials analytical techniques, namely, the Contact Potential Difference (CPD) and the Surface Photovoltage (SPV) for in-line monitoring of both aformentioned damage mechanisms.

CPD measurement employed a vibrating Kelvin probe to measure the difference between the work function of the reference metal probe and the work function of a measured sample. In the case of an oxidized Si wafer, the last quantity was determined by the oxide surface charges[3]. Thus, since the work function of a Kelvin probe was known, CPD provided information about the density of plasma deposited charges that were responsible for antennae damage. Two modes of the SPV operation were employed: the low illumination intensity mode[4] provided information about the minority carrier lifetime in the bulk of Si and about the interfacial recombination velocity at the Si - dielectric interface, and the high illumination intensity mode was used to evaluate charges in the bulk of a dielectric. Since all described material properties strongly depend on defects introduced by plasma radiation, SPV facilitated radiation damage monitoring. Plasma induced defect monitoring was conducted with a commercial, clean room compatible CPD/SPV monitor facilitating fast wafer mapping[5]. Defect mapping capability was particularly important because, in most cases, the mechanism of defect introduction was inherently related to plasma nonuniformities and plasma induced defects were nonuniformly distributed across the wafer. Blank Si wafers (p-type, resistivity = 10 - 20 Ω cm) with thermally grown, 100 nm thick oxides were subjected to a variety of plasma processes compatible with the modern IC manufacturing, and the impact of plasma processing conditions on the SPV / CPD measured plasma damage was investigated. For some of the experiments investigated plasma processes were employed[6] to fabricate test devices (CMOS transistors and antennae capacitors with a 8 nm thick gate oxide). Devices were tested for the capacitor oxide leakage at 3.3 V and the transistor threshold voltage shift.

CPD and SPV mapping showed a strong correlation between the plasma processing conditions and generated defects. For a majority of investigated cases dielectric's surface charging responsible for an antennae damage was the primary source of the plasma induced defects. Fig.1.A presents an example of plasma induced charge distribution on the oxide's surface, and Fig. 1.B. shows the corresponding 3-D projection of capacitor leakage. An excellent correlation between both maps demonstrates that, in the presented case, dielectric charging and

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corresponding antennae damage was responsible for device degradation. However, in many cases both aformentioned damage mechanisms were present. Fig. 2 compares the CPD measured distribution of dielectric's surface charges causing antennae damage, and the SPV measured degradation of the bulk Si and bulk oxide properties due to radiation damage. In this case, device failure is likely to be due to both damage processes. It was also observed that even minor changes in the plasma generation conditions, such as pressure, flow rate, and configuration of magnetic and electric fields could had a major impact on defect patterns observed with CPD and SPV, and the corresponding device degradation.

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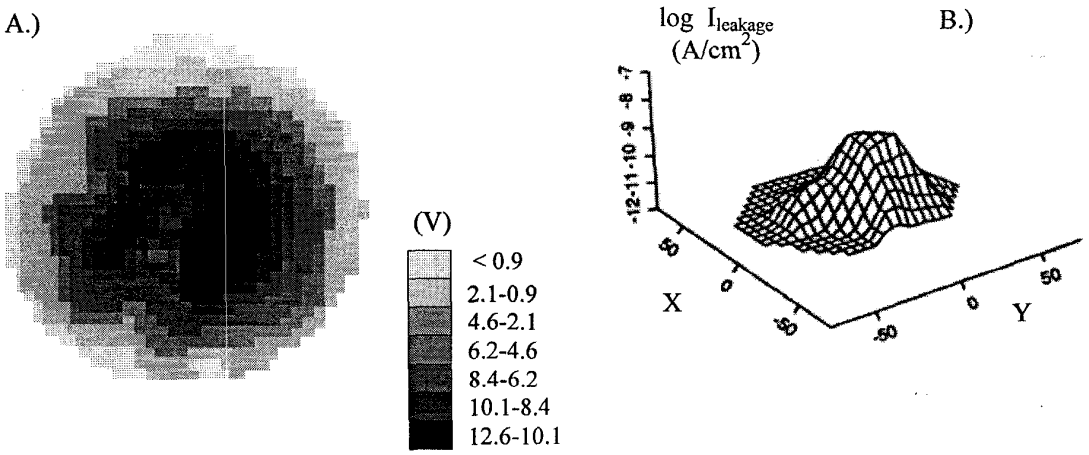

Figure 1. A.) Oxide surface charge maps (CPD units); B.) corresponding maps of the MOS capacitor leakage (80 nm gate oxide). Wafer was subjected to the pre-metal Ar plasma sputtering clean.

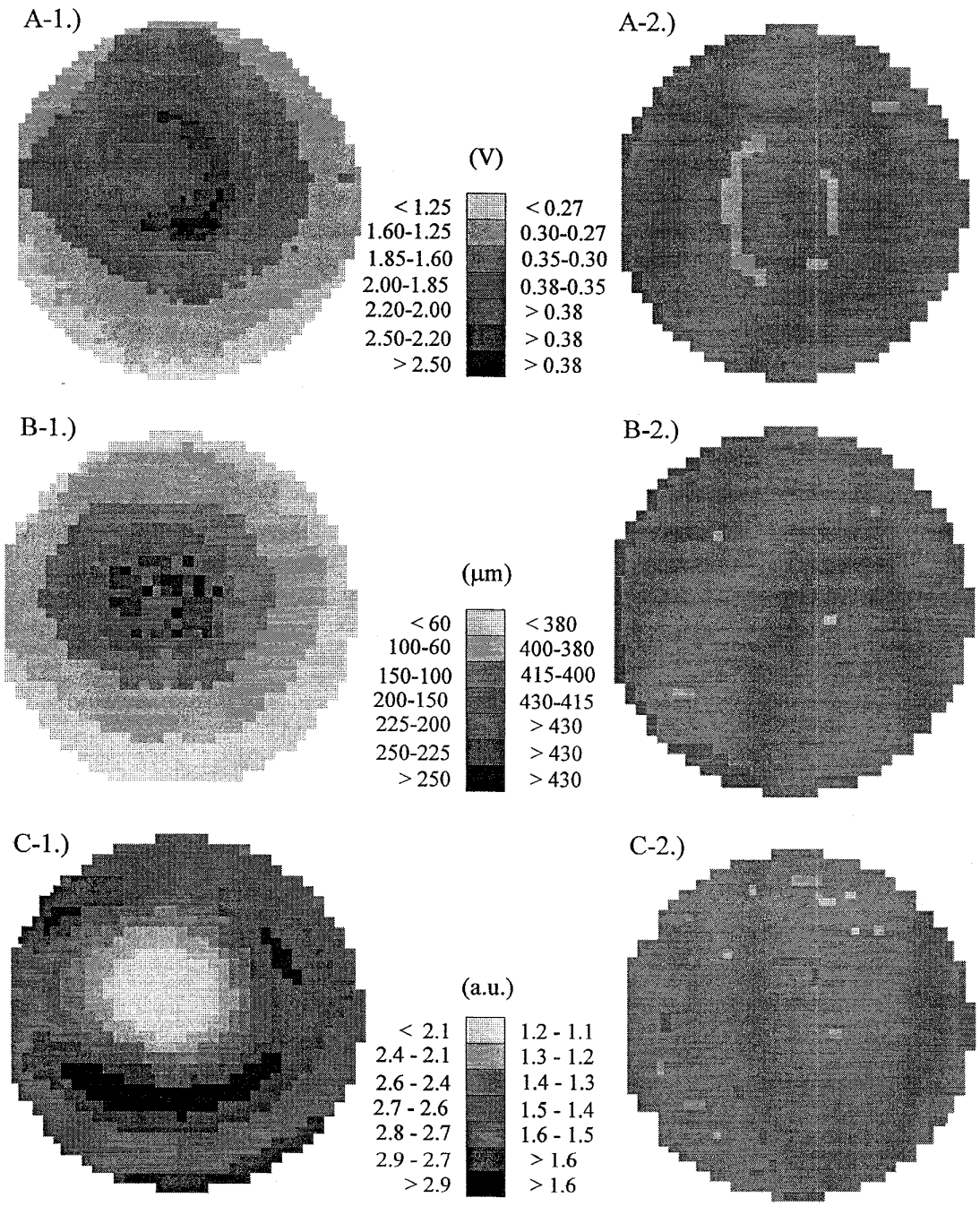

Figure 2. Si wafer after Ar plasma clean: A-1.) CPD map of the oxide surface charges, B-1.) SPV map of the minority carrier diffusion length, C-1.) SPV map of the net bulk oxide charges; A-2.), B-2.), and C-2.) are respective maps obtained for the reference wafers (wafers before plasma treatment).