

# A Complete Approach to the In-line Monitoring of Materials Defects Introduced in Dielectric and Si by Plasma Processing.

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## 1. Introduction.

Fabrication of modern integrated circuits (ICs) involves a large number of plasma processes. They range from cleaning and etching to plasma assisted deposition and implantation. Desired interactions between the plasma and the processed material are often assisted by deleterious processes that lead to permanent and unwanted modification of the device properties. Two major degradation mechanisms are frequently quoted [1]: (1) "antennae damage" resulting from an unbalanced charge transfer between the surface of a dielectric and plasma sheath, and (2) "radiation damage" caused by wafer bombardment by highly energetic photons, ions, and neutral particles originating from the plasma. However, device degradation is frequently a sum of various damage mechanisms, additionally compounded by their interactions during subsequent processing steps and topographical complexity of the processed device structure. Analysis of plasma induced materials defects frequently relies on fabrication of device sensors providing accurate information about specific type of plasma induced defects [2,3]. It is accomplished at the expense of additional devices processing and delays needed for their testing. Purpose of this work is to demonstrate application of a set of relatively simple analytical techniques that can be employed simultaneously providing opportunity for the in-line, real-time monitoring of all types of plasma induced materials defects.

## 2. Experimental Conditions.

Present experiments employed a simple structure (Figure 1) consisting of 1000 Å thick thermally grown oxide on p-type Si substrate (resistivity = 10 - 20 Ω cm). Wafers were exposed to Ar plasma sputter etch process that removed approximately 80 - 100 Å of the oxide. Etching was conducted in Applied Materials P5000 sputter - etch tool employing processing parameters from the range recommended by the equipment vendor. In order to investigate impact of the processing conditions on plasma damage the following conditions were varied: magnetic field (high = 85 G, low = 30 G), plasma generation power (high = 350 W, low = 100 W), and wafer rotation (fast = multiple rotations during plasma process, slow = incomplete rotation during plasma process). Characterization of the plasma induced damage was designed to provide

complete picture of all types of materials defects induced by plasma processing. It targeted defects formed in particular regions (Figure 1) of the measured structure: (A) charge accumulation at the oxide surface, (B) electrical defects induced in the oxide bulk, (C) defects at the Si - oxide interface, and (D) damage induced by plasma in the Si bulk. This task was accomplished with a commercial plasma damage characterization tool [4] combining Surface Photovoltage (SPV) and Contact Potential Difference (CPD) Techniques (Figure 2).

CPD measured ac signal induced by an oscillating shutter between the charged surface of an oxide and reference electrode placed near the oxide surface. This voltage signal can be directly related to the oxide surface charge density [5] ((A) - Figure 1). CPD measured dielectric surface charges has been previously correlated with non-uniformities of the plasma floating potential [6] and with antennae damage in IC devices [1]. The same technique was employed to characterize plasma induced damage in the bulk of an oxide layer ((B) - Figure 1). In this plasma processed wafers were first exposed to a corona discharge. Controlled corona discharge exposure placed desired amount of either positive or negative charges on the oxide surface, and at the same time did not introduced any defects in the underlying oxide or Si. CPD mapping showed that corona discharge provided uniform oxide surface charge coverage (any oxide surface charge non-uniformities induced by the preceding P5000 plasma processing were eliminated during the corona discharge; they could also be removed by dipping wafer in DI water or allowing surface charge dissipate over an extended period of time). Then, wafers were annealed at 150 °C on a hot stage and CPD mapping was repeated. This entire process was an equivalent of the accelerated oxide stressing, with charged oxide surface acting as a biased MOS capacitor plate and wafer's back side held at ground potential. During the heat treatment surface charges dissipated by defect assisted leakage through the oxide. Magnitude of the leakage was related to the local density of oxide defects. Thus, comparison between the CPD surface charge maps before and after anneal differentiated between the regions with large and small concentrations of the oxide bulk defects. SPV was used to characterize Si - oxide interface ((C) - Figure 1) and Si bulk ((D) - Figure 1). High intensity SPV provided information about charges at and in the vicinity of Si - oxide

interface, while low intensity SPV was employed to map distribution of minority carrier recombination centers induced by plasma damage in Si bulk [1,5].

Additional information about plasma induced defects was gained from Deep Level Transient Spectroscopy (DLTS) and C-V measurements. DLTS was used to investigate defects in the Si bulk. It was accomplished using Schottky diodes fabricated on Si after wet etch removal of the oxide. C-V was used to characterize plasma induced electrical defects in the oxide. It employed MOS capacitors fabricated by sputtering Al electrodes on the oxide after plasma processing. Three types of oxide charges were measured: (a) fixed charges, (b) interfacial charges, and (c) mobile charges. Fixed charge ( $Q_f$ ) density was determined from the flatband voltage shift with respect to the theoretical C-V curve [7]. Since this technique relied heavily on tabulated values of Si and Al work functions it was used to evaluate variability of the measured charge at different locations on the wafer rather than for accurate measurement of its value. Interfacial charge density ( $Q_{it}$ ) was measured using the quasi-static C-V technique [8]. Density of mobile charges ( $Q_m$ ) was determined using a routine technique combining voltage stress at high temperature followed by high frequency C-V flatband voltage measurement [9]. Results obtained by C-V and DLTS were correlated with SPV and CPD data obtained at corresponding locations on the wafer.

### 3. Results and Discussion.

Figures 3, 4, 5, 6 demonstrate defect mapping results obtained for the wafer processed under following conditions: plasma power = 100 W, magnetic field strength = 30 G, fast rotation. Figure 4 shows CPD measured bulk oxide defect related leakage under negative and positive surface charge induced bias stress conditions. Similarity of maps in Figure 4 indicates that bulk oxide defects induced by plasma are mostly present in the wafer's center. Corresponding reference wafer maps (wafers measured before plasma processing) were uniform, and they had the following mean values of the measured signal: (1) oxide surface charge (CPD (V)) = 0.24, (2) Si - oxide interface charges (SPV (high intensity illumination) (a.u.)) = 34, and (3) minority carrier diffusion length in Si (SPV (low intensity illumination) ( $\mu\text{m}$ )) = 340.

Change of the plasma parameters did not have significant impact on distribution of defects shown in Figures 3 - 6. It was surprising to find that elimination of wafer's rotation had no impact on defect distribution. However, change in plasma processing condition affected defect mean concentration and distribution uniformity expressed in terms of standard deviation of the measured signal. Figures 7, 8, 9, and 10 demonstrate impact of the plasma conditions on

defects. It appears that decrease of plasma generation power and magnetic field increased number of charges on the oxide's surface and caused formation of a larger number of defects in the oxide bulk. However, larger number of Si - oxide interfacial defects and bulk Si recombination centers were observed when plasma generation power was decreased and field strength was increased. It might be that two different mechanisms are responsible for generation of these two groups of defects.

In order to further elucidate the nature of bulk oxide defects C-V measurements were conducted at locations P1, P2, and P3 shown in Figure 4. Summary of the C-V data is shown in Figure 11, 12, and 13. C-V results are in qualitative agreement with the mapping data in Figures 4 and 5. They reflect non-uniform distribution of oxide defects; ratios of  $Q_f$  and  $Q_{it}$  found in the center (P1) and near the edge (P2) correspond to CPD and SPV signal ratios observed in the corresponding defect maps. In addition, C-V confirmed changes in defect population caused by changing plasma processing conditions. It was also seen that investigated plasma process had no impact on the mobile oxide charges.

SPV measurement demonstrated that plasma processing significantly reduced minority carrier diffusion length. DLTS analysis was conducted to investigate Si bulk defects that might act as minority carrier recombination centers. At least five deep states were observed (Figure 14). Three of them are related to metallic impurities (Fe, Cr, Mo), the other two are probably caused by native point defect complexes that were introduced by highly energetic particles, ions, and photons originating from the plasma. Measurement of defect concentrations and capture cross section indicate that recombination centers related to native point defects are primarily responsible for lifetime degradation.

### 4. Conclusions

Combination of SPV and CPD in conjunction with oxide stressing (employed corona discharge) provided complete information about materials defects induced by commercial plasma process (P5000). It allowed simultaneous and contactless monitoring of defects in four separate regions of the Si - oxide system: (A) charges on the oxide's surface, (B) bulk oxide defects, (C) interfacial charges, and (D) bulk oxide defects. Non-uniform distribution of defects in each of these regions was mapped and related to the plasma processing conditions. Correlation was found between the SPV/CPD monitoring results and more detailed defect characteristics obtained by C-V and DLTS. As previously demonstrated [10] demonstrated defect monitoring can be used to predict plasma related device degradation.

## References:

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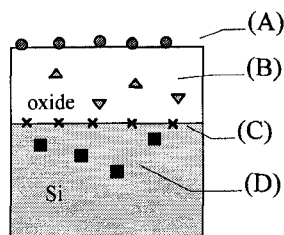


Figure 1. Test structure used in the experiment.

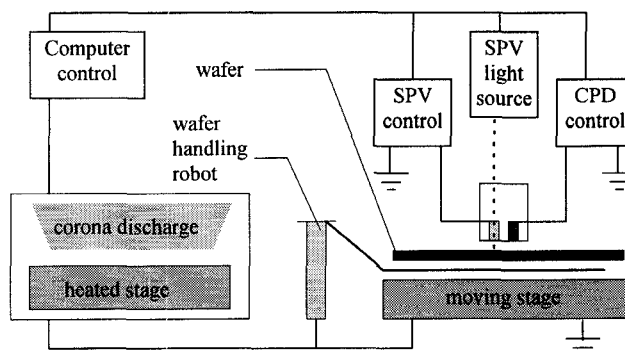


Figure 2. SPV / CPD plasma damage monitoring tool.

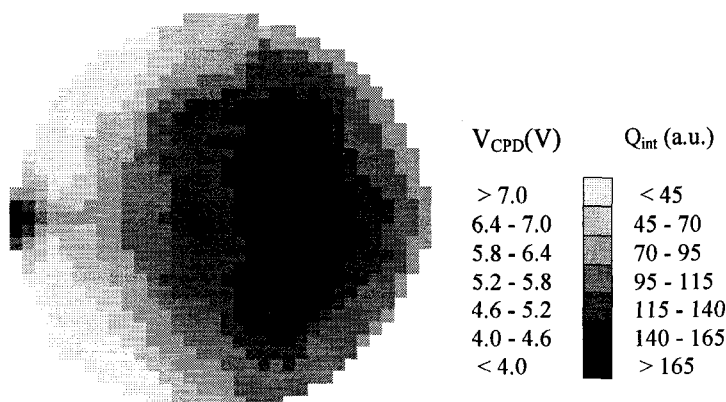


Figure 3. CPD map of the oxide surface charge.

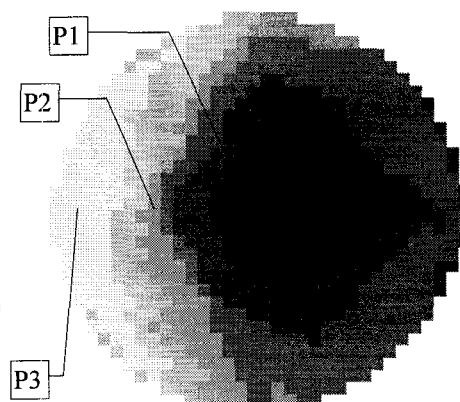


Figure 4. SPV map of charges at and near Si-oxide interface.

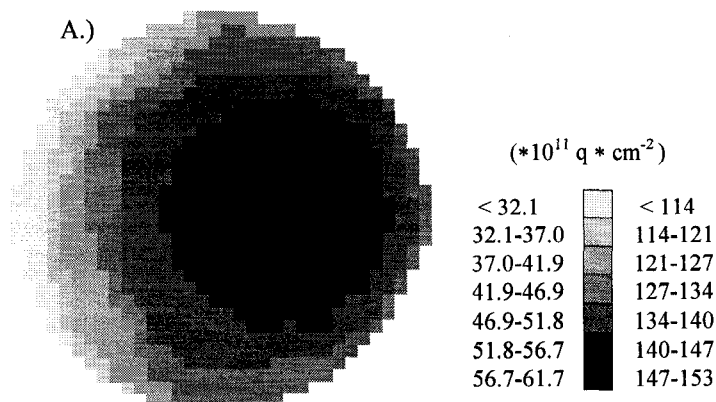


Figure 5. CPD measured change of the oxide surface charge after thermal stress ( $\Delta$  charge) when: A.) charge equivalent of +5.3 MV/cm, B.) charge equivalent of -10.1 MV/cm were placed on the surface by corona discharge.

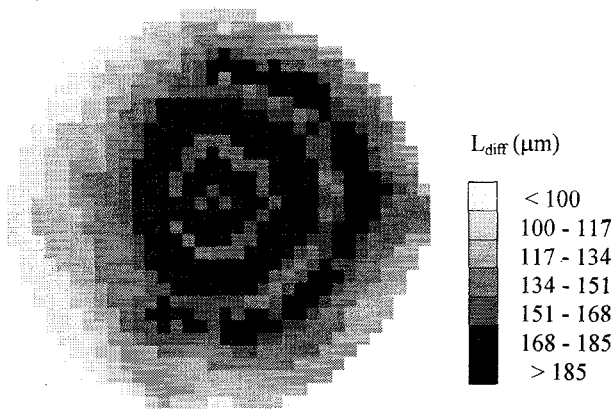


Figure 6. SPV map of the minority carrier diffusion length in Si.

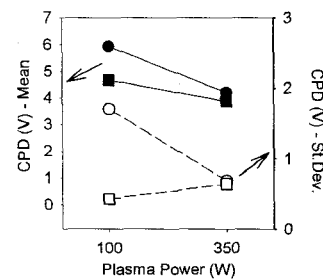


Figure 7. Effect of plasma conditions on CPD measured oxide surface (further explanation - see below).

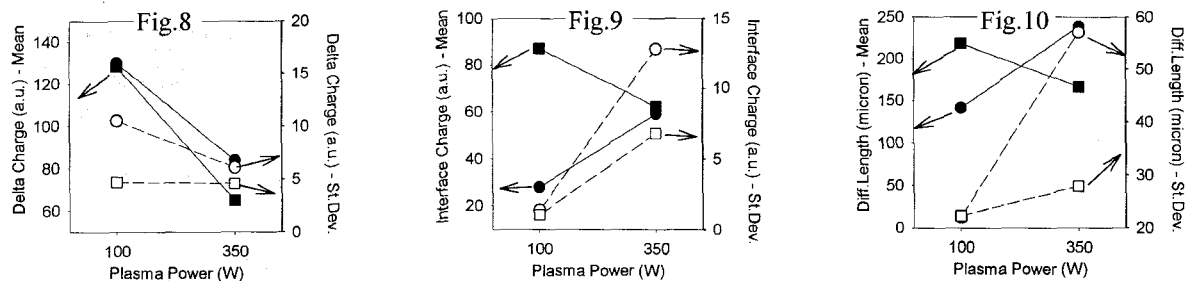


Figure 8, 9, 10. Effect of plasma conditions on defect formation (Fig.8 - CPD measured surface charge change due to oxide leakage (negative bias), Fig.9 - SPV measured Si - oxide interfacial charge, Fig.10 - SPV measured bulk Si minority carrier diff. Length). Circle - magnetic field = 30 G, square - magnetic field = 80 G; black - mean, white - standard deviation.

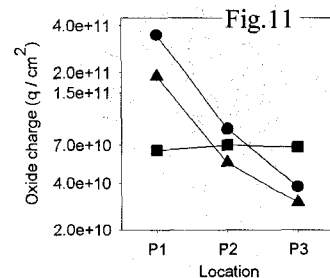


Figure 11. C-V oxide charges (plasma power = 100 W, magnetic field = 30 G). Circle =  $Q_b$ , triangle =  $Q_{ib}$ , square =  $Q_m$ .

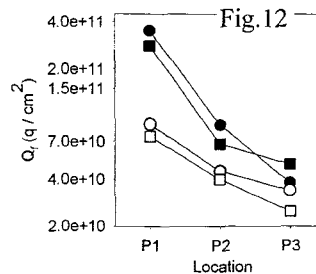


Figure 12, 13.  $Q_f$  and  $Q_t$  as a function of plasma conditions. P = plasma generation power, M = magnetic field strength. Square/black - P = 100 W, M = 30 G, circle/black - P = 100 W, M = 85 G, square/white - P = 350 W, M = 30 G, circle/white - P = 350 W, M = 85 G.

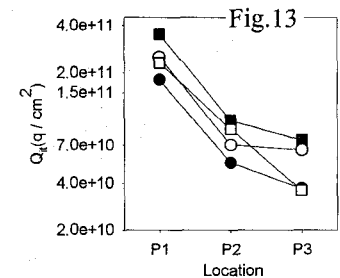


Figure 14:

trap	activation energy (eV)	origin
T1	0.25	Ti
T2	0.28	Mo
T3	0.35	point defects
T4	0.45	Fe
T5	0.5	point defects

