Deep trench fabrication by Si (110) orientation dependent etching

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A simple technique for creating trench structures in silicon using readily available wafer processing techniques is discussed. By using orientation dependent etching of (110) Si, it is possible to create trenches in silicon with vertical sidewalls. The etching anisotropy of certain solutions used with this technique is greater than 600:1 [110]:[111] etching, making it possible to fabricate virtually any value of aspect ratio trench. For this technique, which makes use of two etchants, an anisotropy of 50:1 is demonstrated. The equipment, materials, and processing steps required are outlined. © *1995 American Vacuum Society.*

I. INTRODUCTION

When studying step coverage of deposited films, a common test structure is a trench or groove. It is difficult for most plasma-based etching techniques to achieve 20:1 etch ratios, or have rectangular cross sections.[1–3] Orientation dependent etching (ODE) on the other hand, has the potential to produce a well-defined surface with very large aspect ratios.[4–6] In ODE, a single crystal is patterned with a masking layer and subjected to a surface dependent wet etch. In Si the (111) and (110) planes are the most common for ODE, though some work in producing vertical sidewall etching of (100) silicon has been published.[7] The ODE etch does not attack a particular crystallographic plane as quickly as others [for Si it is typically the (111) plane], producing etching anisotropy as high as 600:1.[5] The (110) wafer orientation is chosen for this work, because the (111) plane lays perpendicular to the (110), allowing for etching of vertical sidewall trenches.

The primary drawback of most ODE techniques for (110) Si is that the base of an etched groove has slanted corners roughly parallel to the {311} planes. The technique described in this paper utilizes two sequential etching steps that produce a highly anisotropic etch with trench bases perpendicular to the sidewall. The technique produces a trench with a rectangular cross section and can be fabricated in virtually any desired aspect ratio.

II. EXPERIMENTAL EQUIPMENT AND MATERIALS

The technique involves minimal equipment, most of which is readily available. The only specialized equipment is a photoresist spinner, a contact mask, and a thermal oxidation furnace. Other equipment includes ovens for soft and hard baking of photoresist, an alignment fixture for holding the mask in contact with the wafer, a temperature-controllable, heater-jacketed Pyrex bath with a water-cooled lid, magnetic stir bars, a hot plate/stirrer, and various Pyrex and Teflon beakers capable of holding the wafers. The materials required include (110) lightly doped silicon wafers ($\rho \geqslant 0.1\ \Omega$ cm), photoresist, photoresist developer, hydrofluoric acid (HF 50% in H_2O), ammonium fluoride (NH_4F 40% in H_2O), concentrated sulfuric acid (H_2SO_4), 30% hydrogen peroxide solution (H_2O_2 that is *not* stabilized is preferred, stabilized H_2O_2 contains tin), potassium hydroxide (45% KOH by weight in H_2O), and isopropyl alcohol.

III. PROCEDURE

When reading this procedure, there are a few items to keep in mind. First, any mention of water for mixing solutions or rinsing means deionized H_2O. For mixture recipes, the proportions are volumetric, unless otherwise stated. Finally, after each step involving an aqueous mixture, the wafers should be rinsed in deionized H_2O for 5 min then blown dry with a moisture-free and oil-vapor-free gas.

A photomask of the desired pattern is needed for pattern development on the masking layer. The one used here is designed for trench production, and consists of 1.041 cm by 0.512 cm die patterned in chromium. Each die consists of 74 sets of five trenches, with 5, 10, 15, 20, and 30 μm widths. They are separated by 10 μm lines that are the silicon walls after processing. The trenches and walls are aligned with the 0.512 cm direction. Eight test patterns are dropped in around the periphery and in the center of the wafer for quantification of the etch process (see Fig. 1). Dimension tolerance, photoresist exposure, wafer orientation marks, and 66 sets of trenches make up the features of the diagnostics die.

The first step is to create the masking material on the cleaned silicon wafers. A thermally grown oxide or nitride is required. The layer needs to be thick enough to last until the end of the second KOH etching step. A 7600 Å wet silicon oxide layer is grown at ~1000 °C on 3-in. (7.5 cm)-diam boron-doped (110) Si wafers. To estimate the thickness of the masking layer required, the observed oxide etch rate in the KOH baths is abut 10 Å/min. Including all process steps, a 1000 Å would have been sufficient in this example. The silicon:silicon dioxide etch selectivity for the entire process is about 3000:1.

Once the masking layer is grown, it needs to be patterned. Shipley 1813 photoresist is applied to the wafer, then it is spun at 3500 rpm for 30 s. The wafer is then softbaked at 95 °C for 30 min. After the photoresist is softbaked, the wafer is mounted in the mask alignment fixture. The fixture consists of two aluminum frames that can be tightly clamped together. On one-half of the fixture there is an opening so that the photomask is fixed in it with epoxy mounting seals.

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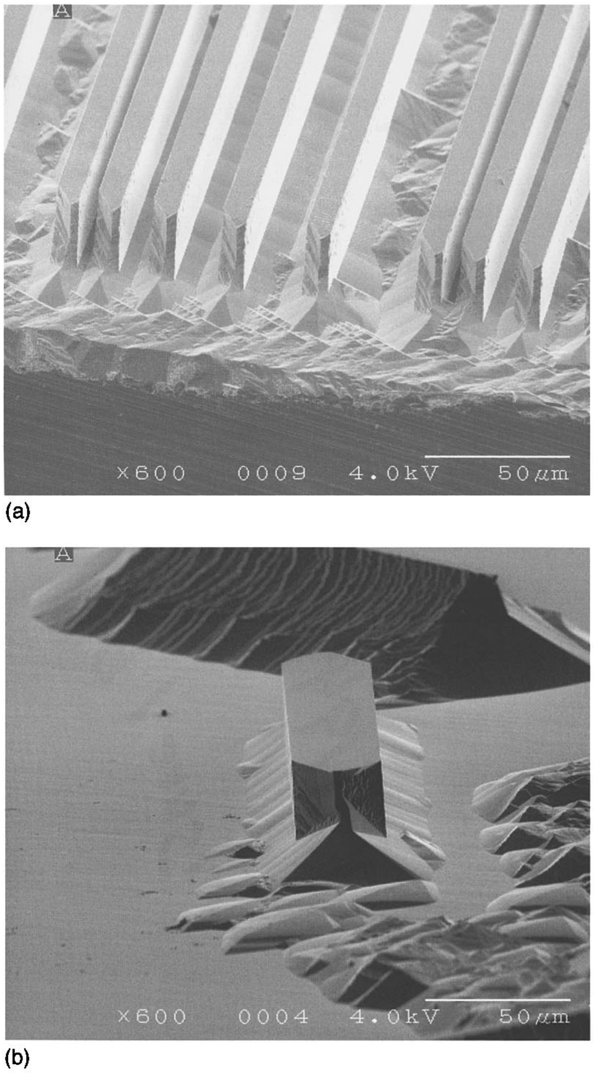

FIG. 1. (a) Scanning electron microscopy secondary electron image of etched trenches using 80° 45% KOH in H_2O for 5 min. (b) Scanning electron microscopy secondary electron image of etched mesas using 80° 45% KOH in H_2O for 5 min.

The tolerances between the alignment pins and fixture holes should be as small as possible to minimize slippage. The wafer should be oriented such that a 35.3° counterclockwise angle between the wafer flat and the desired patterned mask lines is formed. This is a critical step, since the degree of misalignment determines the amount of anisotropy achieved, and the microscopic roughness of the sidewalls. A tolerance of ±2° is found to be adequate for the process, though alignment within ±1° is routinely achievable. When the fixture is clamped together, the photoresist should be in contact with the photomask everywhere on the wafer. Any gaps will lead to poor image registration. The wafer is then exposed to the ultraviolet (UV) light source. Exposure time will have to be determined for each process, but the exposure used in this case is 26 s for a Model 23 Optical Associates light source in a Model 750 Optical associates mask aligner. It is important to make sure the wafer is at a constant distance from the light source to minimize exposure variation.

Photoresist developing is done in a 5:1 H_2O: Shipley 351 Microposit developer for 45 s. (The developer is a NaOH, surfactant, H_2O mixture.) It is hardbaked at 140 °C for 30 min. After this coating, a backside coating of photoresist is applied with another hardbake. The backside coating is used to preserve the back side oxide. The wafer is then placed in a buffered oxide etch (BOE) for 10–11 min, or until the wafer becomes hydrophobic, to etch through the oxide masking layer. A $HF:NH_4F$ 1:11 solution is used to inhibit swelling and liftoff of the photoresist. The photoresist is then stripped in a Piranha etch of concentrated H_2SO_4:30% H_2O_2 at 6:1, heated to 120 °C. (Depending on the hydrogen peroxide temperature and age, it may not be necessary to apply an external heat source.) It is recommended that the hydrogen peroxide be refrigerated when not in use to prolong its lifetime. The solution will turn yellowish once the wafer is added to the solution, but will become clear once the photoresist is fully removed. A thin oxide layer will form on the silicon during the photoresist strip, so it is necessary to place the wafer in the BOE for 30 s to remove the layer.

The next two steps are the most critical of the fabrication process: the two KOH etches. The temperature tolerances are very tight, because the etch rate can vary by more than 5000 Å/min within a 10 °C range. Therefore it is recommended that a ±1 °C tolerance be maintained. The first etch is 45% KOH by weight in H_2O heated to 80 °C. The solution is placed in a heat jacketed Pyrex bath with stirring capabilities. The bath needs to be covered to minimize fluid evaporation. A water-cooled lid is recommended for fluid retention. Stirring of the solution needs to be active enough to keep the solution thoroughly mixed to minimize thermal and concentration gradients (120–150 rpm). Place the wafers in the bath only after it has reached its proper temperature. The etch rate is about 3 μm/min with a typical anisotropy of 150:1. After the etch the trench sidewalls have been formed. The sidewalls are perpendicular to the face of the wafer after this etch, but between the bases and the sidewalls are slanted faces that are parallel to the (311) plane and protrude about 20 μm from the sidewall [see Figs. 1(a) and 1(b)].

The second etching step uses a 25% by weight KOH in H_2O. The purpose of this etch is to remove the slanted faces at the bottom of the trench. Once the KOH solution is in the bath, a 5 cm layer of isopropyl alcohol is added to it. The alcohol forms an immiscible layer on top of the KOH solution. The alcohol can be mixed into the KOH by stirring at about 120–150 rpm. The alcohol boils at 84 °C, so it is critical that the bath always be kept below this temperature, though the operating temperature of this bath is 80±1 °C. The bath needs to be stirred such that the alcohol layer is mixed with the H_2O. Wafers need to be spaced such that they receive adequate circulation of the solution. The etch rate is 2500 Å/min, but the anisotropy is only 6:1 (see Fig. 2). This etch attacks the slanted faces very effectively, and completely removes them within 5–10 min. Longer etching risks overetching in the lateral direction.

The last step is to remove the remaining masking oxide. Typically 10–15 min in the BOE solution will suffice. The wafer is rinsed for 5 min in H_2O and then blown dry. After this step the process is complete (see Fig. 3).

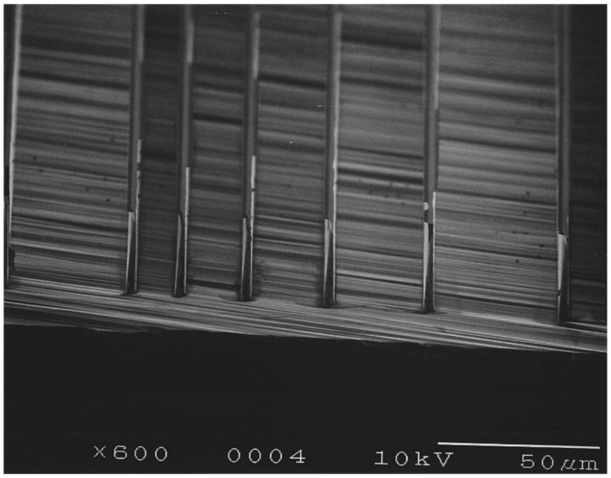

FIG. 2. Scanning electron microscopy secondary electron image of etched trenches using 80° 25% KOH in H_2O and isopropyl alcohol for 120 min.

IV. RESULTS

Figure 1 shows the effects of the 80 °C KOH, H_2O etch on (110) Si with the (111) aligned masking layer. The trench walls are perpendicular to the (110) plane, and the etch rate is about 2.5 μm/min. For the sample shown in Fig. 1(a), the anisotropy is about 150:1, however, the trenches have slanted bases. Other samples show trenches as deep as 40 μm, with widths of 5 μm. Examining Fig. 1(b), in which there is more than 100 μm between the walls, it can be seen that the slanting face does not intersect the (110) plane. By measuring the angles between the (111) and (110) planes with the slanting plane, it is seen that the slant is about 32° from the (110), and about 58° from the (111) face. This coincides with the (311) plane intersecting the (111), and (110) planes. These slanting layers are also seen for closely spaced grooves etched into (110) silicon by Bean and Kendall.[5,6] Also, the ends of the trenches have been etched into other planes. The plane of the ends of the trenches is (112).

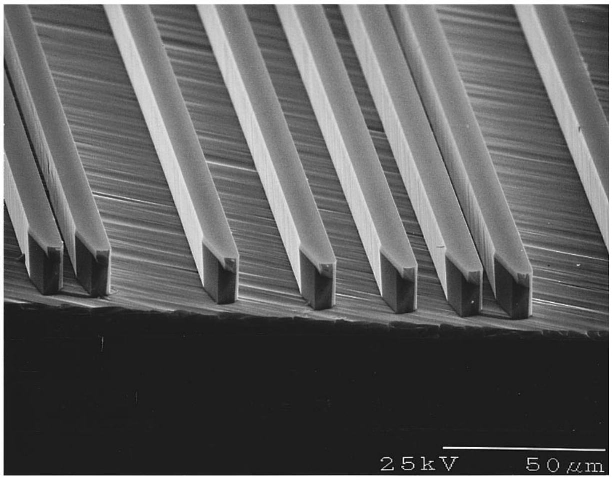

FIG. 3. Scanning electron microscopy secondary electron image of etched trenches using a combination of the two etchants, each for 5 min.

Figure 2 shows the effect of the KOH/H_2O/isopropyl alcohol etch on another wafer. The sidewall etching is much more pronounced, and the anisotropy is about 6:1 with an etch rate of about 2500 Å/min. However, the most important feature to note is the absence of the slanted plane. It is not possible to see the slanted plane under any magnification. The etch rate of this process is similar to that measured by Price under similar conditions.[8]

By combining the two etches, it is possible to get the best features of both etches. The KOH/H_2O etch is applied to create the trench, with KOH/H_2O isopropyl alcohol to remove the slanted plane at the bottom. The result of the two-step etch is shown in Fig. 3. The overall process anisotropy is about 50:1 for the silicon. Of course this will vary to some degree depending on the relative etching times of the two solutions. One problem encountered during etching is that the 5 μm trenches experienced a slightly lower etching rate of about 3%. This is probably caused by poor fluid transport within the trench. It should be noted, however, that poor stirring during the second etch will destroy the patterned features. Therefore, spacing of the wafers in the bath and the degree of mixing must be carefully adjusted and maintained.

V. SUMMARY

A wet etching technique for etching perpendicular full-rectangular cross-section trenches in silicon using low cost materials and equipment has been presented. As shown in the micrographs, it is possible to produce a trench with perpendicular sidewalls with a flat base. The key to success of the technique is the combination of the two etches, such that the anisotropy of the first etch is not lost during the second etch, but that the length of the second etch is sufficient to remove the slanted plane material. The slanted plane appears to be a nominally (311) plane. The technique has been successfully used to develop trenches of many different aspect ratios with trenches as deep as 40 μm and as narrow as 5 μm. If care is taken with mask alignment, etch baths temperature, and agitation, then it is possible to achieve a flat-based trench with perfectly vertical sidewalls.

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