LEAKAGE CURRENT BEHAVIOR IN COMMON I-LAYER A-SI:H P-I-N PHOTODIODE ARRAYS

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ABSTRACT

Hydrogenated amorphous silicon photodiode arrays form the basis of monolithic three-dimensional integrated circuit sensor technology. In these arrays, the intrinsic a-Si:H layer covers the entire area to maximize light collection. One technique by which the pixel diode is defined, is to pattern the bottom contact layer independently of the intrinsic layer. One of the most important characteristics of any diode array, however, is that the dark-state reverse bias leakage currents must be as low as possible to minimize diode noise. This study examines the leakage currents associated with the pixelated array. These structures are unique in that the edge of the diode is defined by the local electric field between diodes, rather than the physical surface of an a-Si:H film. The effect of the diode edge has been found to induce a field-dependent component to the reverse bias leakage current. For example, diodes with 5500Å i-layer, have a junction leakage of 14 to 20 pA/cm^2, at 5.0 x 10^4 V/cm, while the pixel edge-dependent current component can be as high as 30 pA/cm^2. In addition, it will be shown that the i-layer thickness and junction doping plays a key role in determining the behavior of the leakage currents.

1 INTRODUCTION

Over the last ten years, there has been increasing interest in the use of a-Si:H in photodiode arrays that are monolithically integrated onto integrated circuits [1-3]. Such integration allows a combination of 1) reduced imaging pixel area, 2) reduced sensor cost, 3) lower photodiode leakage, and 4) improved pixel sensitivity. As pixel-level complexity (hence area) grows, the advantages become more apparent. In order to maximize the photodiode light collection area of the array, the array is designed to have a continuous fully depleted intrinsic layer, and patterned electrodes on the integrated circuit side of the pixel to define the diode. One of the most important performance requirements of any imaging array is the dark-state reverse bias pixel leakage current, (a.k.a. dark current), as this sets the lower limit of dark spatial noise (shot noise). In most designs, the photodiode junction leakage current is a limiting factor, therefore, it is worthwhile to minimize this value. For a-Si:H photodiode arrays, leakage current sources include 1) junction leakage, 2) thermally generated bulk currents, 3) array edge injection currents, and 4) pixel edge leakage currents. Some work has been done on characterizing junction, bulk, and array edge injection currents for stacked diodes, however, little if any has been said about the pixel edge currents due to the difficulty of pixel fabrication [4-6]. It has been widely assumed though, that for the p-i-n diode stack, edge currents are dominated by surface states along the junction boundary. However, since that these diodes have continuous intrinsic layers, it is possible to decouple the effect of the of a-Si:H surface states from the edge of the array. This gives a unique opportunity to examine purely geometric effects of the pixel edge. The objective of this paper is to explore the diode edge effects on leakage current behavior as a function of electric field, i-layer thickness, and contact layer doping.

2 EXPERIMENTAL

Details of diode fabrication have been presented elsewhere, and are only briefly described here [1, 2, 7]. Diode array fabrication starts with a standard integrated circuit process flow. The photodiode array consists of n-type a-Si:H pixels overlapping a thin metallic pixel contacts with a common intrinsic and p-type a-Si:H layers that form an array of p-i-n junctions, (see Figure 1). Top contact to the array is made by using a transparent conductor layer that connects the top surface of the p-type a-Si:H layer to vias adjacent to the array, (monolithic top contact structure) [2]. Allowing the transparent conductor to be in contact with the edge of the intrinsic layer for the array simplifies sample construction, but puts the transparent conductor in direct contact with the intrinsic layer [1, 8]. This produces a contact junction that injects a dark current into the array, which overwhelms any surface state leakage formed by the physical array edge. However, all test structures are bounded by a ring diode that is held at the same bias as the measurement structure itself, so that it removes the injected current.

The test structures measured for this paper came from a general process development vehicle design for this process flow and consists of junction area ranging from 140 μm on a side up to 1940 μm on a side, and striped pixel-edge intensive structures with 940 μm sides ranging from 3.7 x 10^3 μm, to 1.2 x 10^6 μm. Two series of samples were made: 1) various i-layer thickness 3000, 4000, 5500, 7500 and 9000Å, 2) where the p-layer boron atomic concentration, was varied from 7.0 x 10^{19} cm^{-3} to 2.1 x 10^{20} cm^{-3}, and the n-layer phosphorus concentration was varied from 2.0 x 10^{20} cm^{-3} down to 2.0 x 10^{19} cm^{-3}, all measured by SIMS. In all samples the rest of the p-i-n junction stack contained a p-layer thickness of 200Å, an n-layer thickness of 500Å, and a 600Å transparent conductor layer on top of the p-layer. The a-Si:H layers are formed by very high rate PECVD deposition methods (> 20 Å/s), with the resultant films having an intrinsic defect density of < 4 x 10^{15} cm^{-3} [9]. Unless otherwise noted, the dopant concentrations of the junction layers are: [B] is 7.0 x 10^{19} cm^{-3} for the p-layer, and [P] is 2.0 x 10^{20} cm^{-3}, for the n-layer.

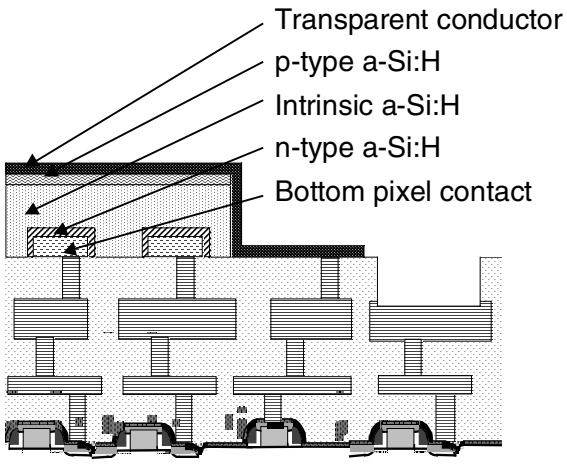

Figure 1: Schematic diagram of elevated a-Si:H photodiodes.

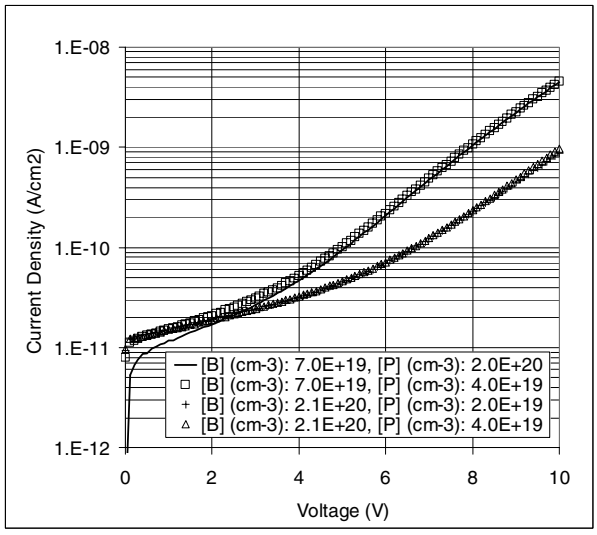

Figure 2: Reverse dark J-V plot of a-Si:H p-i-n junctions with various p- and n- doping concentrations. The i-layer thickness is 5500Å.

Two types of electrical measurements were made on the devices utilizing an Agilent 4156B. One was a reverse bias I-V measurement, in which the junction bias was varied from 0 to either 5 or 10V reverse bias in 0.1 V increments. At each measurement point, the measurement was made after a 65 second hold at bias and a long measurement integration time, thus allowing for 40fA sensitivity. The other was a low frequency transient decay measurement made under reverse bias conditions from 0.2 to 4V. In these experiments, the instrument was put into a sampling mode in which data was collected every 0.1s, and the current was monitored from the point at which the diode bias was switched from 0V to the set bias. In all cases, the guard-ring diode that surrounded the structure-under-test was driven with identical voltages but utilizing separate source measurement units, so that there was no current flow between the two devices. All measurements were made in complete darkness and a sample temperature of 21°C.

3 RESULTS

The effect of p and n layer doping levels on current density is shown in Figure 2. In this case, the solid curve has the same doping level as the thickness series experiment and each junction had an i-layer thickness of 5500Å. The J-V of Figure 3 shows two leakage current behaviors, with a transition point about that increases with i-layer thickness. Given the dopant concentrations in each junction, there is a correspondence of phosphorus doping and the low bias region in which the higher phosphorus concentration corresponds to lower junction leakage. Conversely, the boron doping concentration correlates to the higher bias region, in which higher boron concentration leads to lower junction leakage.

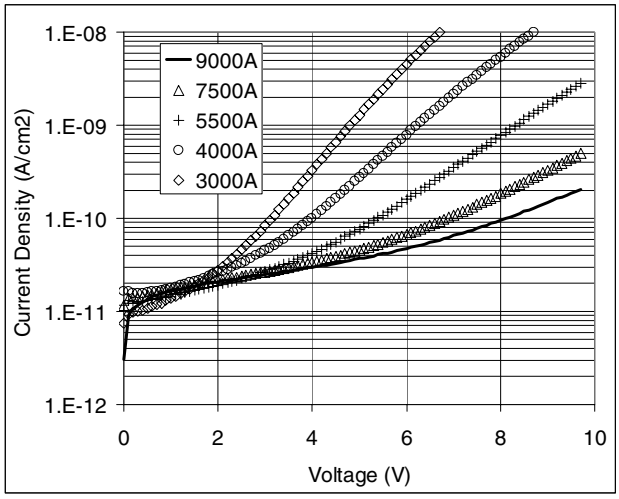

Figure 3: Reverse dark J-V plot of a-Si:H p-i-n junctions with various i-layer thickness.

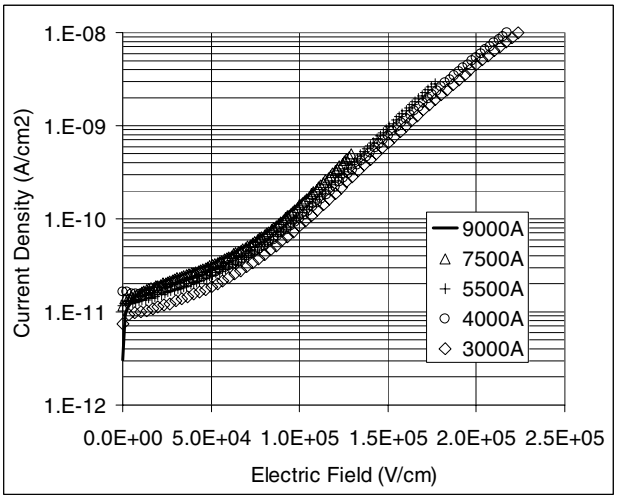

Figure 4: Reverse dark J-E plot of a-Si:H p-i-n junctions with various i-layer thickness.

The reverse bias junction current density behavior of a 940 μm x 940 μm square diode as a function of i-layer thickness is shown in Figure 3. For each curve the junction shows qualitatively the same behavior, with a relatively voltage independent regime at low biases, then switching to more voltage dependent regime at higher voltages. The lower voltage regime is largely independent of thickness. For the 9000Å diode, the junction shows full depletion above 300 mV, even though the p-layer is only 200Å thick, and that point of full depletion decreases as the thickness decreases. At 1V reverse bias the current density is about 15 pA/cm^2, and at 2V it is about 20 pA/cm^2. Figure 4 shows the same data re-plotted for current density as a function of electric field. This plot demonstrates that the thickness dependence is largely related to the

applied electric field, and shows that the critical electric field between the two current density regions is about 7 x 10^4 V/cm.

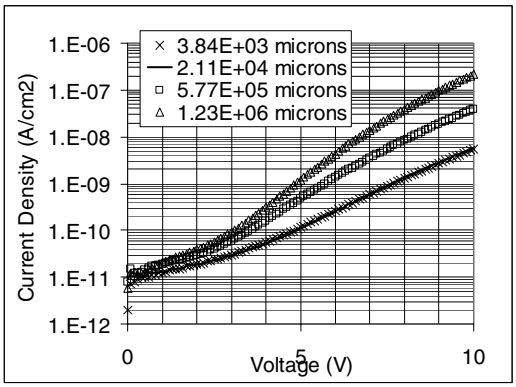

Figure 5: Effect of pixel edge length on J-V. The i-layer thickness is 5500Å.

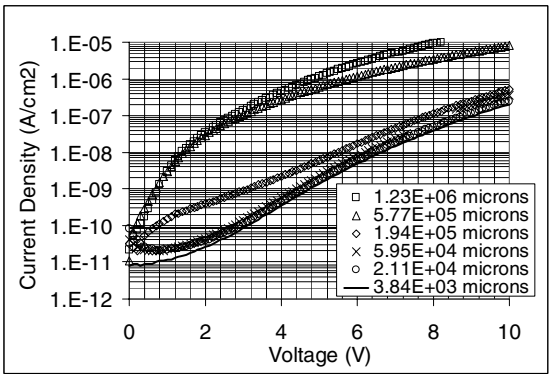

Figure 6: Effect of pixel edge length on J-V. The i-layer thickness is 3000Å.

While previous work by Schiff [4] and Street [5] have studied the effect of the diode stack edge length on reverse bias leakage current densities, Figure 5 shows the effect of the length of the pixel edge length, in which the edge terminates within the i-layer itself, on the leakage current density for a 5500Å thick i-layer. The leakage current density seen here is representative of the diode leakage seen in arrays that share a common i-layer. Figure 6 shows the effect of pixel edge length with a 3000Å i-layer. For short pixel edge lengths, the behavior shows a low bias voltage independent regime and an exponentially increasing high bias regime. As the pixel edge length increases, there is a decrease in the transition bias between the low and high bias behavior, until the low bias behavior is completely suppressed. For the longest pixel edge length devices an almost linear regime occurs at higher biases. In all cases, though the overall leakage current increases as a pixel edge length increases. At modest voltages, the change in leakage as a function of pixel length can result in a 1000x increase in leakage current.

Figure 7 is a plot of the transient leakage current density plot for a 5500Å thick i-layer p-i-n diode upon switching from 0V to 0.2, 1 and 4V reverse bias from 0 to 300 s. The plot shows that the current decay time is largely independent of the bias, though the steady state leakage increases as a function of reverse bias. It also shows the transient behavior when switching from 0 V to some applied bias appears that by 300s, the steady state current has not yet been reached. The 65s hold time was selected as the maximum clock time allowed by the instrument, and shows that its value is about 2x higher at 65s than at 300s for all values. Therefore, the behavior seen at 65s is directly proportional to that 300s. For the 1V reverse bias condition Figure 7 shows that the decay current is roughly 12 pA/cm^2 at 300s. The 0.2V bias shows 4 pA/cm^2, though this is for a non-fully depleted situation. In addition, there is no evidence of a long-term increase in the leakage current, which has been attributed to reverse bias injection across the junction contacts [10]. It has also been shown that the decay transient is independent of junction dopant concentration.

Figure 8 is a log-log plot of the leakage current density as a function of electric field, the same data as shown in Figure 4. Above 7 x 10^4 V/cm, all curves for all thickness i-layers follow the same exponential behavior. Below 7 x 10^4 V/cm though, for diodes, except the 3000Å one, show a slight but increasing field dependence as a function of field. The 4000Å thick diode

shows no field dependence. The low-field dependence shown in Figure 8 is evidence that there are two distinct mechanisms driving the leakage current.

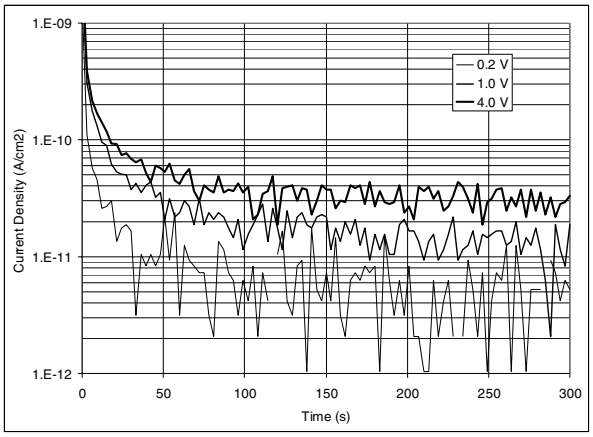

Figure 7: Current decay plot for 0.2, 1, and 4V reverse bias. The i-layer thickness is 5500Å.

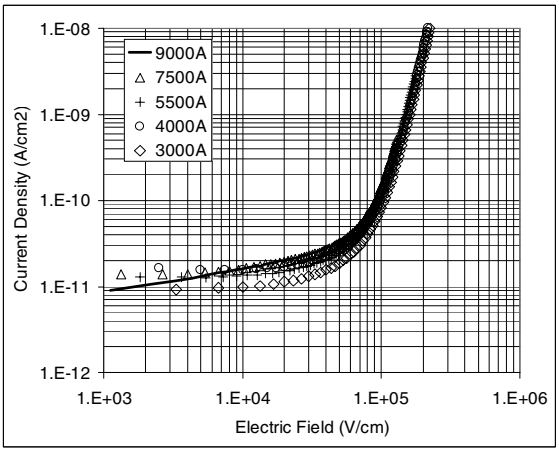

Figure 8: Reverse dark log J- log E plot of a-Si:H p-i-n junctions with various i-layer thickness.

4 DISCUSSION

The junctions presented here appear to push the quality given the leakage current densities and thickness of the p-layer. Work by Street has shown that previously, high-quality junctions with 500Å thick, doped layers and 1 micron i-layers fully deplete around 0.7 V, and have about 15 pA/cm^2 leakage currents at 2.0V [5]. The junctions created for this work were optimized for maximum quantum efficiency with a 200Å p-layer, however the diodes were fully depleted at 0.3 V, and a 20 pA/cm^2 after 65 s at 2.0V. Given the ~33% drop in leakage current density between 65 and 300s, the long-term steady-state value would be close to 14 pA/cm^2.

It is generally believed that the cause of time dependent behavior of a-Si:H p-i-n junctions is governed by leakage across the doped junctions, and thermal current generation [5, 10]. Thermal current generation alone cannot account for the field dependent behavior seen in the J-V plots, so most invoke a Poole-Frenkel effect. Ilie, however, has shown through calculation that the Poole-Frenkel effect does not account for the strong field dependence, and proposed instead an electron-lattice interaction mechanism [6]. This phenomenon is a tunneling phenomenon in which the tunneling rate is strongly dependent upon the carrier effective mass, and the electric field.

The effect of pixel edge length on J-V behavior also appears top be field-dependent. MEDICI finite element analysis of the pixel edge region shows a higher electric field than the region toward the pixel center, even when only 1 micron from adjacent pixels of an identical potential. To first order the effect is likely largely dependent upon the area ratio of p-type and n-type contact layers. Therefore, the increase in pixel edge length increases the applied electric field at the pixel periphery thus inducing higher field behavior than for area diodes. The form of the J-V plots is therefore a summation of low and high field regions within the pixel.

The behavior of the J-V curves as a function of junction dopant concentration is very interesting in that low bias behavior is governed by the n-layer doping, and the high bias behavior is governed by p-layer doping, and can be explained by the electron-lattice mechanism. Given the high doping density of the junctions the depletion depth into the junctions varies by about 10Å/V. Therefore for the p-layer, there still exists at least 100Å of non-depleted material at 10V. Therefore, it is unlikely that across junction leakage contributes. On the other hand, the

defect pool model can be used to explain the doping dependence. The defect pool model suggests that the position of defect states within the gap near an interface is influenced by the local Fermi level [11]. If the depth from the interface of intrinsic material influenced by the contact layer Fermi level is greater than the carrier diffusion length, it can be expected that the effective mass will change correspondingly. Thus increased doping of the n-layer increases the valence band defect density of the interfacial i-layer thus increasing the e- effective mass. electron-lattice coupling and hence the tunneling rate will change. It is therefore likely that the low-field behavior seen in Figure 8 is due to the Poole-Frenkel effect, while high field behavior is caused by deep-state tunneling [6, 11, 12].

5 SUMMARY

This work has detailed the leakage current density behavior as a function of junction dopant concentration, pixel edge length, and i-layer thickness. I-layer thickness does not affect current leakage other than by modulating the electric field for a given potential. The high junction doping shows no evidence of the contact layer injection currents, even though the p-layer is only 200Å. This allows the steady state leakage current at 2.0 V to be as low as 14pA/cm^2. Also, it has been demonstrated that the pixel edge does contribute to increased leakage currents even when adjacent pixels are held at constant voltage. It appears that the cause is field-enhanced emission. Since it appears that the interfacial a-Si:H region may well govern the leakage current, it will be necessary to take steps to control the evolution of these states during growth. Finally, it has been proposed that the low-bias behavior is governed by the Poole-Frenkel effect, while the high bias behavior is caused by electron-lattice coupling driven tunneling, can be modulated by deep-level interfacial states derived in response to the local Fermi level.

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