Advances in elevated diode technologies for integrated circuits: progress towards monolithic instruments

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Abstract: Integrated circuit manufacturing capabilities have reached the stage where it is technically and economically feasible to create new components that may be monolithically combined with them to create unique devices. One of the most elementary yet reliable of such monolithic components is the elevated diode. These diodes may be used to detect or generate light for parallel photodetection or photogeneration applications, such as imaging, chemical detection, or displays. Because new materials are required for all implementations, various process flows and integration challenges are discussed. In particular, focus on interconnection to the top and bottom of the junction is considered. In addition, since the elevated diode concept gives the designer control of such parameters as junction thickness, semiconductor bandgap, and light emission spectrum, the issues that drive junction design are presented for both the elevated photodiode and elevated OLED. Finally, because of the decoupling of diode size and pixel size, and the presence of new materials, novel pixel circuits are considered to achieve novel or greater pixel-level functionality, and because material behaviour may dictate the method to drive the junction. The new possibilities that these junctions present create a new realm of applications and are initial examples of a new class of devices called monolithic instruments.

1 Introduction

In the 1950s when Kilby and Noyce developed the concept of the integrated circuit, they ushered in the second generation of semiconductor devices based upon increasing levels of functional integration. Undoubtedly, the integrated circuit has profoundly changed world society by the development of new types of components for applications that could not exist without them. In addition, the manufacturing infrastructure that has been created to produce these components is the most highly precise, large volume manufacturing system ever devised. Single crystal silicon wafers and the miniaturised devices created on them are among the most precisely manufactured objects in production today. By leverage this manufacturing platform, it is possible to create new devices that were unheard of just a few years ago. One class of newly emerging devices are array-based sensors, most of which are based on photon detection. Given the ease of adding photodiode and photogated structures, integrated circuit technology readily lends itself to the design and manufacturing of such devices. Photosensing is the most pervasive detection technique applied to a variety of phenomena including spatial imaging, motion detection, chemical analysis, thermal mapping, navigation, biometric analysis, etc. [1–3]. Since 1990 interest has been rapidly growing in developing these devices as an alternative to CCD-based image sensors because of the high level of functional integration, unique methods of sensing element (pixel) readout, and low power that may be achieved [4, 5]. In the course of array sensor development, primary issues include dealing with trade-offs between pixel area, pixel-level functionality, array size, cost, and perhaps most importantly, photodiode area.

One of the most intriguing concepts is one in which the elements of the pixel circuit are extracted from the c-Si substrate and placed on top of the integrated circuit. In these concepts, a layer of semiconducting material is placed above the interconnect structure of the integrated circuit to typically create p-i-n or p-n diode junctions, creating completely monolithic three-dimensional semiconductor circuits. For example, a-Si:H has been used to create photodiode arrays on top of CMOS sensors arrays [6–9]. Elevated photodiodes arrays provide four unique capabilities that are not matched by crystalline silicon photodiode devices: (i) the ability to separate photodiode design and placement from other pixel circuit elements; (ii) the ability to maximise light collection area within the array; (iii) the ability to engineer the semiconductor to precisely tailor spectral response; and (iv) the ability to create multijunction or multiple layers of diodes to collect several portions of the electromagnetic spectrum. The performance and cost advantages that can be realised by elevating the photodiode array encourages increasing pixel functionality so that several different pixel architectures have been developed for use with them. Beyond sensing, organic light-emitting devices (OLEDs) have also been placed onto integrated circuits to create emissive microdisplays [10–12]. This article discusses state-of-the-art of elevated diode technologies, their current projected applications, and future prospects for these technologies. It also points out that what arises from the elevated diode technology is the first appearance of a new class of devices called monolithic instruments. Monolithic instruments are systems that contain standard

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electrical integrated circuit components and new functional components, are able to interact with their surroundings in ways other than electrically, and are fabricated using a single semiconducting substrate.

2 Elevated diode technology

2.1 a-Si:H photodiodes

Crystalline silicon photodiodes are the current mainstay of integrated silicon photodetectors. They typically consist of p-n junctions in the silicon substrate on which no silicide has been formed. Their main advantage is that they are a by-product of standard processing in which the only additional processing is to create a silicide blocking layer, and perhaps a few optimised implants. While these features make it extremely simple to integrate, there are several problems with their use. The main disadvantage is the trade-offs between crystalline photodiode area with other circuit elements within each pixel. Typically, size optimisation is the trade-off in sensitivity with noise suppression. Other issues affecting sensitivity include the depth of the optical well within which the photodiode is contained. As device process technologies scale to smaller dimensions, part of the scaling is realised by the addition of more interconnect metal layers. Interconnect routing is constrained to maximise light collection by the photodiode. Scaling increases the depth of the physical well in which the photodiode is placed. In some cases, this tunnel can be 10 μm long for a diode that may be only 4 μm wide. While resist-based microlenses placed over the pixel increases light sensitivity, when combined with the light tunnel of the interconnect the acceptance angle is severely reduced. This means subsequent imaging optics require a high degree of telecentricity, thus raising optics complexity and cost.

Elevated photodiodes have several advantages over photosensors embedded in the silicon substrate. These include finer resolution, greater light collection area, more efficient photosensitive layers, and less light dispersion from intervening layers. An example of these advantages can be seen in Fig. 1. Here the three-transistor (3T) source follower pixel architecture is implemented in the same process technology: Fig 1*a* shows a crystalline Si photodiode; and Fig. 1*b* is an elevated photodiode. In this instance a 50% pixel and array-area reduction is realised, but the photodiode now collects light over 100% of the array. Finally, since the photodiode is on top of the sensor, the optical acceptance angle is maximised. Several attempts to create elevated photodiode arrays on CMOS and CCD technologies have been demonstrated based on hydrogenated amorphous silicon (a-Si:H) as the semiconductor [6, 7, 9, 13–16]. Acceptance has been slow due to potentially expensive manufacturing techniques because of low a-Si:H deposition rates, difficulty in maintaining clean junction interfaces, complex upper contact schemes, and difficulty in controlling pixel isolation. However, recent work has shown that these structures can be made cost effectively and enhance overall imager performance [6, 7, 16].

2.1.1 Junction technology: In any sensing system maximising the signal-to-noise ratio (SNR) is normally the most important consideration. Since the sensor is the first stage in the system, the theoretical SNR limit for the system is set at the pixel. When designing the p-i-n junction to maximise SNR, there are two considerations: maximising the quantum efficiency (QE) for the wavelengths of interest to boost the signal, and minimising the dark leakage current to help determine the noise floor. There are several techniques to improve both parameters, but of course these solutions often improve one factor at the expense of the other, so trade-offs are necessary.

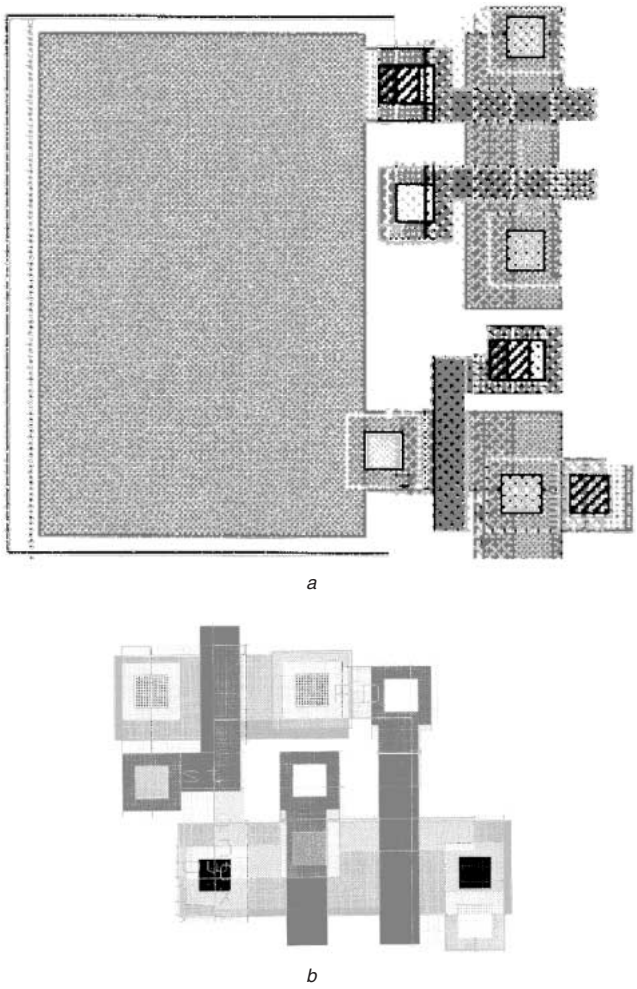


Fig. 1 *Junction and polysilicon layout of 4.9 μm three-transistor (3T) pixels*
a Image of a conventional crystalline Si photodiode
b Layout of an elevated photodiode structure, showing approximately 50% pixel area reduction by removal of the crystalline Si photodiode

The performance of a-Si:H p-i-n diode arrays is normally better than standard crystalline silicon diodes, especially in terms of absolute quantum efficiency (QE) and junction leakage current, the two most important diode parameters. Two approaches that have been implemented to maximise QE include thinning the non-depleted layer of the p-i-n junction, and minimising the absorption of the upper-doped layer through bandgap widening. In the visible range, a-Si:H p-i-n QE varies from 40% around 450 nm, 83% at 570 nm, and 20% around 700 nm (see Fig. 2). The short wavelength QE is largely dependent upon the depletion depth from the topside of the diode which can be modulated by the upper layer doping concentration and thickness, while the long wavelength QE is controlled by junction thickness and carrier lifetimes, though for high-quality a-Si:H below a few microns, carrier recombination is negligible. Figure 2 shows the effect of p-layer thickness on light collection efficiency. Going from 200 Å down to 100 Å significantly increases short wavelength QE by a factor of two. The use of p-type a-SiC:H as the top contact layer has been used to maximise light collection [17, 18]. a-SiC:H conductivity is lower than a-Si:H for alloying contents of less than 20% C, while it increases the bandgap by 0.25 eV. Increasing the C content above 20% leads to higher defect

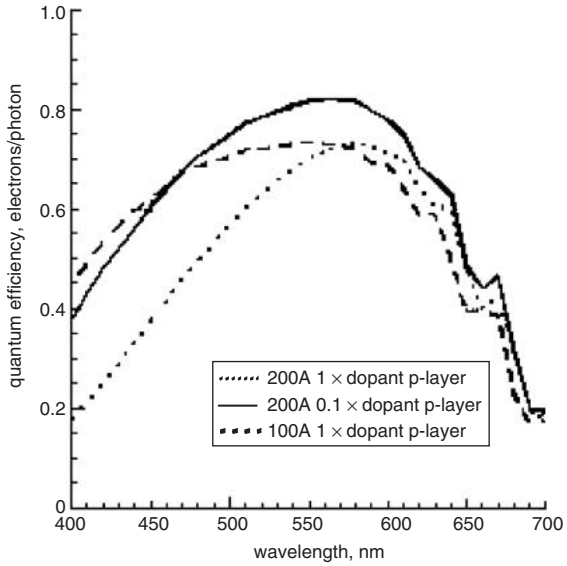


Fig. 2 *a-Si:H photodiode quantum efficiency collected under −2.5 V bias*

densities and an increase in dark currents. The wider bandgap has lower optical absorption and can lead to a 20% improvement in QE.

Diode leakage currents are controlled by the trap state density, carrier thermal generation rate, and contact layer injection. Since the bandgap (more accurately known as the mobility gap) consists of a continuum of localised states, localised state depopulation leads to a time-dependent decay current [19]. For moderate fields ($\sim 10^4$ V/cm), it can take more than 300 s for the leakage current to reach steady state, as shown by the current decay of one of the diodes, shown in Fig. 3. The steady-state current arises from thermal generation from the localised states. However, if the dopant concentration is low enough, as states in the intrinsic layer depopulate, the applied field extends further through the doped layer, eventually initiating injection currents from the metallisation layers, and a corresponding current increase [19]. As Fig. 3 shows, contact injection does not occur even as high as 10 V, indicating that contact layer doping is sufficiently high.

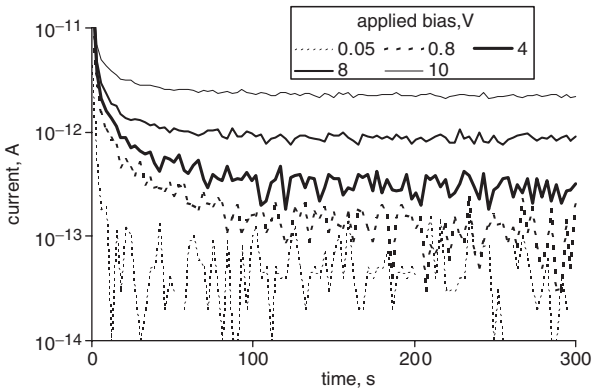


Fig. 3 *Effect of applied bias and measurement time on a-Si:H p-i-n diode junction leakage current*
Intrinsic layer thickness is 9000 Å

The temporal effects of localised state depopulation require special care when optimising p-i-n parameters. Inadequate hold times for I–V measurements can provide misleading information, if the sampling time is not chosen correctly, since the leakage current is a function of both applied bias and time. However, when trying to characterise the diode leakage current for use in a sensor, delay times on the order of the actual integration time should be used to gain insight into diode operation under real conditions.

Figure 4 is a series of dark I–V measurements as a function of intrinsic layer thickness taken with a 60 second delay time at bias before each measurement, which provides values within a few per cent of the steady-state value. Not only does junction thickness affect diode QE, it also has an effect on the diode baseline dark current. Figure 4 shows the effect of junction leakage for various i-layer thicknesses. Each curve shows phenomenologically the same behaviour, in that the leakage exhibits a small-exponent power law increase, then switching over to a higher increase rate at larger bias. Typically, most p-i-n junctions show a region of extreme voltage dependence at low bias, <0.7 V, which has been attributed to creation of a fully depleted junction [20]. However, as shown in Fig. 4, each junction is fully depleted by 0 or 0.1 V, thereby implying that the built-in field is sufficient to fully deplete the junction. Even though the p-layer is only 200 Å leakage current are 2.3×10^{-11} A/cm^2, at 2.5 V, and about 1.5×10^{-11} A/cm^2 at 1 V. It is interesting to note that the leakage current at low bias is largely independent of the intrinsic layer thickness. It has been suggested that for such low leakage currents the main generation mechanism are the deep-level states within the intrinsic layer, implying that the steady-state leakage current should be proportional to thickness [19, 20]. Since it is thickness independent, it implies that the leakage current may be controlled by another source, so it can be argued that further reductions in the steady-state leakage current are possible. Additionally, as the diode thickness decreases, the inflection point voltage decreases and the exponent increases suggesting electric field dependence.

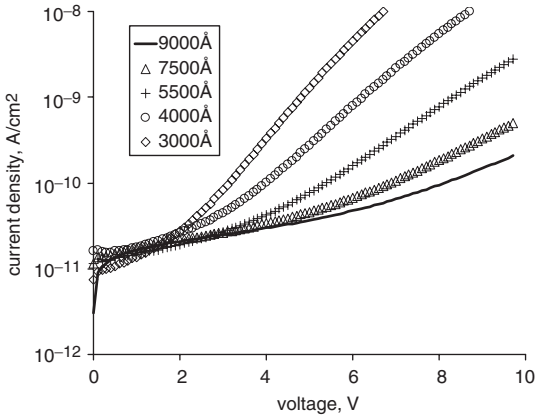


Fig. 4 *Leakage current density as a function of junction bias for different intrinsic layer thickness*
The heavily doped layer thicknesses were 200 Å p-layer and 500 Å n-layer. The measurement conditions were 65 s hold before each measurement, in 100 mV steps

The current leakage behaviour of one of Agilent's diodes (a diode with monolithic top contact and a top conductor that makes contact to the i-layer at the edge of the array) is shown in Fig. 5. Because of the intimate contact between the top conductor and the intrinsic layer a large injection current flows into the array at this point and is drawn off using a guard-ring, shown in Fig. 5*a*. The device has three connections, the top contact COMMON, the central diode (CTR), and the guard-ring diode, (R1). By driving CTR and R1 at the same bias, no current flows between them, and the guard-ring collects the entire array edge leakage

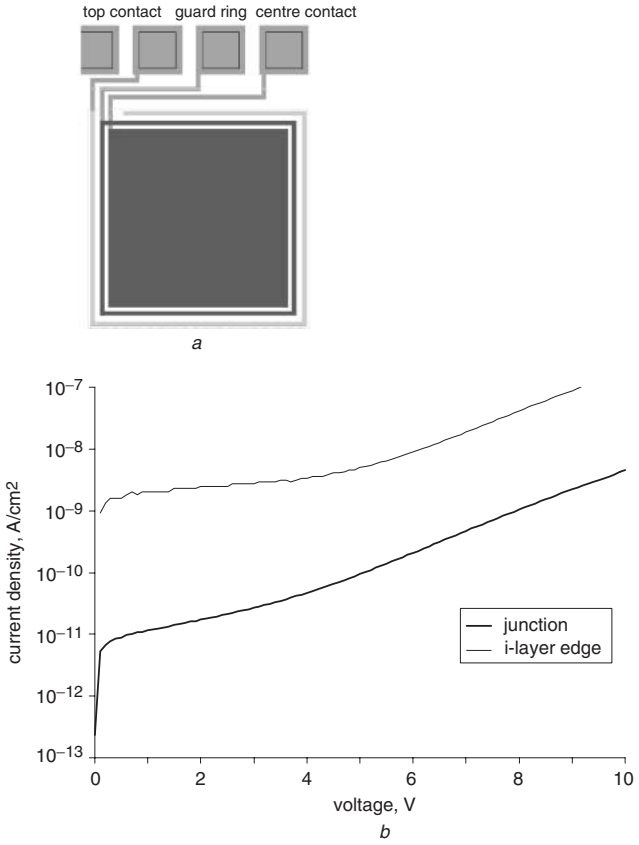


Fig. 5 *Current leakage behaviour of test structure*
a Test structure to measure dark leakage current density
b Dark current density leakage as a function of applied reverse bias, for 1 s hold times, 5500 Å intrinsic layer thickness, and a junction area of 0.0025 cm^2

current. The guard-ring is 10 μm from the array edge and 5 μm from the central diode. The reverse bias curve shown in Fig. 5*b* shows the current density calculated from the two current components. The array edge leakage current density is denoted in Fig. 5*b* as J_{edge}, it is a current density with the area defined as the product of the array edge perimeter and the intrinsic layer thickness, and is about 2.5×10^{-8} A/cm^2, about 10^3 times higher than the junction leakage current density. This shows that the guard-ring does indeed successfully remove all of the edge injected current, in actual arrays; such currents have never been seen more than four pixels from the array edge under normal operating conditions.

From the previous discussion it is clear that to a large extent diode performance is governed by balancing p and n contact layer doping and thickness, and potentially the intrinsic layer thickness such that the steady state leakage current is at the desired value for the maximum operating potential. Therefore from a junction optimisation perspective, maximising the intrinsic layer thickness will minimise dark leakage current. At the same time, it is critical to minimise these values to improve short wavelength QE. As long as high quality material can be deposited with good junction interfaces, it has been clearly demonstrated that high performance junctions can be readily created.

Ensuring high-quality a-Si:H p-i-n junctions means that the single most critical steps in elevated photodiode array production are the a-Si:H depositions. Since it is critical to create clean junction interfaces within the p-i-n stack, the methods used to deposit that stack have influenced the device architecture chosen by various groups. In addition, the characteristically low deposition rate normally assumed to be required to produce high-quality a-Si:H in parallel plate PECVD reactors has also been considered to be a major limiter in minimising production costs. The reasons have been that parallel plate PECVD processes were considered to be too slow to be viable and other plasma source configurations had yet to be proven production worthy. Over the last few years though, it has been found that high quality material can be formed at deposition rates that had not been considered possible before. Theil *et al.*, have created a process that produces an intrinsic film with a defect density of about 4×10^{15} cm^{-3} and a deposition rate about 25 and 30 Å/s [14, 21]. They found that by keeping the transit time through a plasma short, and the partial pressure of SiH_4 low, it was possible to deposit the films at pressures of several Torr, and power densities of a few tenths of a W/cm^2. Matsuda describes a different approach in which the ideal method for maximising the deposition rate and producing high-quality material is to maximise the SiH_4 flow, minimise reactive radical production, and keep the partial pressure and power density low [22]. In both cases, it is felt that the high-quality material is made by preventing the incorporation of multi-silicon clusters into the evolving film. As long as cluster formation is suppressed, film quality will be relatively immune to increases in deposition rate.

2.1.2 Structure and process technology: Elevated photodiodes are p-i-n junctions fabricated from semiconducting films that are deposited on top of the integrated circuit. The three main technical issues when developing elevated photodiode arrays are providing a proper passivation dielectric between the standard integrated circuit and the elevated diode array, ensuring sound contact to the integrated circuit, and adequate pixel definition/isolation. Contact to the bottommost terminal is readily achievable, however, making contact to the top of the device without (i) blocking light, (ii) making an unreliable connection, or (iii) using a cumbersome fabrication scheme is not as straightforward. Pixel isolation is the degree to which individual pixel diodes in the array are electrically or optically separated from one another. While it is necessary to isolate certain elements of the diode junction to define the area of a pixel, some components such as the intrinsic layer of the diode may connect pixels. The primary advantages of the continuous intrinsic layer are that it maximises light collection area, which is especially important when the pixel area/edge ratio is small, and it simplifies manufacturing. On the other hand, a continuous intrinsic layer may allow unacceptably high charge transfer between pixels, which compromises signal integrity.

The base on which the photodiode array is constructed is the integrated circuit passivation layer. This material serves two purposes: to protect the integrated circuit underneath, and to provide a mechanical base for the construction of the photodiode array. Therefore these layers must provide adequate adhesion to the diode and contact layers. In addition, it has been found that the layer needs to be planarised to improved the general light collection properties of the sensor array. While it has been argued that a non-planar topography for the photodiode maximises the light collection area, experience has found a few disadvantages of the non-planar surface. The first is that the surface scatters more light between pixels. This can enhance optical crosstalk between pixels which translates into greater optical noise. For example, in a colour sensor, the sharing of light between different coloured pixels reduces the colour space separation of the pixels. Another factor is that diode

topography requires a greater depth of field in focusing, increasing the minimum lens/sensor spacing that is achievable. The two methods to minimise such effects are to planarise the passivation dielectric [23], and use polished metal vias, such as those made from the W CVD/CMP process flow.

There are two distinct architectures by which contact can be made to the top contact of the diode stack: monolithic and external contact. Monolithic contact involves making the connection between a deposited transparent conductor and the interconnect by way of vias or exposed metal regions. The strap can be either a separate metal film or the transparent conductor itself. The strap must be deposited onto both the top of the diode array and the integrated circuit interconnect to one side of the array. At the edge of the array, it has been considered desirable to ensure the isolation between the strapping conductor and the array edge by use of insulating films. Array edge isolation requires additional masking steps to define robust contact.

Such complexity and cost may be avoided by allowing the strap to short circuit the edge of the array. The short circuit injects current into the array (which can be of the order of 10 nA for a 1 cm × 1 cm array), but by relying on guard-ring diodes to draw off the injected current, there is no performance degradation. Allowing the strap to short circuit the edge of the diode array reduces the mask count by two with respect to the isolated strapping approach. This is a key point as the two-mask reduction can reduce the cost of the array fabrication by roughly one third. Since the guard-ring is only required at the array termination, it is usually an acceptable trade-off between array size increase and process complexity.

The other top contact architecture is based on external wiring. These techniques include wire bonding, solder bumping/flip-chipping, or mechanical contact to the transparent conductor on top of the diode array. However external wiring (i) requires additional process development at the point of product packaging, (ii) does not allow product testing prior to packaging, and (iii) increases product yield loss at packaging; thereby making it an undesirable technical path. For example, wire bonding would require room on the array to accommodate a mechanically sound landing pad. To date, there has been no public claim of implementation of this technique.

In addition to making electrical contact to the common topside of the array, it is also necessary to make bottom-side contact to each pixel. Most implementations of the elevated photodiode have been n-layer on the bottom [24, 25]. It is an advantage for this layer to be highly reflecting in the wavelength range of interest so that for more weakly absorbing wavelengths, >570 nm, the optical path through the diode is doubled. There are two demonstrated approaches for connecting the bottom-side pixel contact layer to the interconnect: (i) one in which the via fabrication is compatible with high-density interconnect techniques (metal/CMP method), [6, 7], and (ii) the other where a shallow slope contact allows direct contact between the interconnect metal and the bottom layer of the pixel (direct pixel contact method) [26]. Theil *et al.* first employed planarised vias, with the goal being reliable and compact vias that minimise the amount of pixel area consumed by its presence [6]. Here vias are made by standard logic CMOS integrated circuit process modules in which a TiN-clad tungsten metal contact is formed through planarised passivation layers. At the end of the standard CMOS process flow, the passivation layer is planarised and a contact hole is etched through the dielectric. A TiN adhesion layer is deposited in the vias, then the vias are filled with W from a high-step coverage W-CVD deposition process. Construction of the vias is completed by chemical mechanical polishing (CMP) to remove the excess W and TiN, leaving W-filled vias. When using a 0.35 μm process, the vias can be about 0.5 μm in diameter and take up about 1 μm^2 area (including design-rule based isolation). They typically have a resistance of 3–4 Ω. It is also possible to use more advanced interconnect metals, such as Cu-based vias. Such vias would be produced by a single damascene process flow after passivation planarisation. A completed cross-section of the monolithic elevated diode array with planarised via is shown in Fig. 6, which was fabricated in a 0.35 μm process.

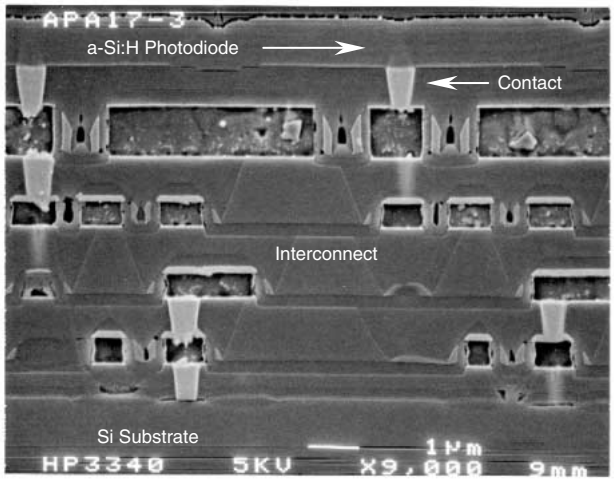


Fig. 6 *SEM cross-section of elevated photodiode*

The other pixel contact structure is the direct pixel contact. The essence of this technique is to etch a via through the passivation dielectric to expose a landing pad on the top metal level in the interconnect. The contact film and p-i-n diode are deposited into this via such that they are in direct contact with the metal landing pad. The advantage of the technique is that it requires fewer processing steps than the planarised via method, however, since the deposited films that make up the diode stack have very poor step coverage, the via sidewalls must be very shallow to permit adequate coverage. In the LARS II pixel layout, the via accounts for about 2.5% of the pixel, or a via that is 6.3 μm in a 0.8 μm process technology. While this area is relatively small for the large pixel, it would not be acceptable for smaller pixels such as the 3T design. For a 3T design implemented in a 0.35 μm process, the pixel size is about 4.9 μm to 5.9 μm on a side, so accommodating a direct pixel contact via would require more than doubling the pixel area. Scaling the larger LARS II pixel from 0.8 μm down to 0.35 μm process technology does not reduce the via size, thus for a 5x pixel area reduction, the proportion of the pixel taken up by the via pad increases to about 13%.

Pixel definition allows spatial separation of collected light even though the light collection region is usually continuous. Several methods have been proposed and/or implemented based on the degree to which various components are isolated and the process flow used to achieve the isolation. These methods include: (i) self-aligned, (ii) patterned pixel, and (iii) isolated diode techniques. Each process flow has its own combination of advantages, such as low cost, simplified processing, minimal junction interface exposure, minimal topography, good electrical isolation, and minimal process variance.

The simplest technique is the self-aligned pixel definition process. In this case the pixel is defined after deposition of the bottom pixel contact layer by etching a deep trench into the passivation dielectric thus self-aligning the bottom contact layer with the pixel edge [25]. Then all three p-i-n layers are deposited in a single pumpdown, thus preventing contamination of the internal p-i-n junction interfaces. Pixel isolation relies on poor step coverage of the doped layers to break electrical continuity between pixels. The advantage of this process flow is that it is very simple and low cost, however, there are several drawbacks. First of all, the passivation dielectric must be thick enough to accommodate a deep enough trench to create the isolation. This can push the planarised pixel contact process capability, and increase the direct contact via dimensions. Also, interpixel leakage can be high and have a large variance (i) if the bottom doped layer severance is difficult to achieve, and (ii) if trench profile variation significantly affects deposition topography. Another potential issue is that since the trench is employed to prevent continuous film growth, the a-Si:H that grows from the sidewall of the trench can be quite different from the a-Si:H on the planar surface, which may create issues with electrical performance. For example, the plasma density on the sidewall will be much lower than on the planar face. If the growth process for high-quality film relies upon the energy produced by ion bombardment, then the sidewall material will be inferior.

Another approach to pixel definition is one in which the bottom contact layer and the bottom p-i-n junction layer are patterned prior to deposition of the rest of the diode stack, and is referred to as the patterned pixel definition technique [6, 7]. In this process flow, the pixel is formed by standard photolithographic techniques and is then either wet or dry etched. Once the resist has been removed, the intrinsic and upper-doped layer stack is deposited. This flow is more complicated than the self-aligned flow, but has distinct advantages with respect to topographic control of the pixel profile. By minimising the overetch of the passivation dielectric, there will be less sidewall deposition in the intrinsic layer of the diode. In addition, there will be less demand on the dielectric thickness margin, thus allowing greater design flexibility in interconnect specifications. Also, the minimal overetch required minimises issues with across-wafer etch profile variation, which governs all subsequent depositions. The two ways in which the diode patterning may be accomplished is by either etching both the bottom contact layer and the bottom junction layer at the same time (self-aligned), or by patterning them separately (double-etch). The self-aligned approach is less costly, and can potentially introduce less vertical topography. However, depending on the work function of the bottom contact layer and its electrical separation from the intrinsic layer, it may introduce an undesirably high leakage current into the diode. The double-etch approach requires two separate patterning and lithography steps, the bottom junction layer overlaps the bottom contact layer on all sides. This introduces additional topography and process complexity, however, it ensures electrical isolation of the bottom contact layer and the intrinsic layer, thus minimising dark current.

A third type of pixel definition structure that has been proposed is the isolated diode technique. In this class of structures, each pixel is isolated from other pixels by a dielectric layer [17, 23]. There are two ways in which this can be implemented. One way is to deposit the bottom contact layer, and p-i-n stack (or at least through the intrinsic layer), then etch the layer, and backfill it with dielectric [23]. This is a very attractive approach in that it will provide complete pixel isolation and is self-aligned. In terms of process cost and complexity, it has the potential to be simpler than the previously discussed structures. However, the drawbacks are that the array no longer provides 100% optical layer coverage, the intrinsic layer now has physical interfaces that must be properly handled to avoid edge leakage, and additional processing is required to ensure that diode top-contacting is reliable. The other approach is one in which diode area is patterned into the passivation dielectric prior to layer formation [17]. In this approach, the diode is formed into the pixel. Though it is not clear how the pixel separation is achieved, a couple of techniques include (i) a patterned etch of the p-i-n layers on top of the isolation dielectric, and (ii) CMP of the raised regions. Afterwards, the common electrode layer is deposited. It was shown that crosstalk between pixels was suppressed by at least 95%. Depending on the application, such suppression may or may not be acceptable.

Once passivation, contacting, and definition/isolation have been achieved, the basic technology for elevated diodes is in place. However, since it is possible to engineer more than a single p-i-n junction, one can consider alternative sensing designs including engineered spectral response through bandgap engineering, and multispectral junctions. These are junction capabilities which are just not possible with the substrate-based photodiode pixel. The amorphous silicon-based system has been shown to have optical sensitivity from the near-UV (a-SiC:H) to the near-IR (a-SiGe:H) [27, 28]. In order to achieve good UV response, Mutze *et al.* re-engineered the photodiode to include a-SiC:H for both the upper p-layer and the intrinsic layer, which allowed them to achieve a peak QE of 40% at 400 nm, and as much as 20% QE at 350 nm [27]. Therefore it is possible to specify the bandgap and thickness to control long wavelength cut-off. It is also possible to specify the non-depleted layer thickness on the light input side to control short wavelength cut-off.

Most photosensor arrays are planar in that they have a single junction per pixel. To detect colour, a colour filter is placed over each pixel. Typically, three separate colours are used, and reconstruction of a full colour picture occurs by a process called demosaicing. Demosaicing algorithms seek to reconstruct a full colour map from the incomplete chromic/spatial data set provided by planar sensor arrays where each point can only detect a single colour. These techniques usually take up more processing power and die area than any other aspect of the image pipeline. An architectural advantage of the elevated photodiode is the ability to stack multiple junctions on top of one another. This allows for multiple wavelength detection at a given point that makes possible more accurate colour and spatial reproduction, i.e. the elimination of demosaicing. The drive architecture of stacked diodes will be determined by how many terminals and their location in the stack. Several approaches have been implemented or proposed, including various two- and four- and six-terminal multiple diode stacks to achieve three-colour detection [25, 29, 30]. One such design is the p-ii-n-i-p two-terminal diode stack [29]. Because of the junction symmetry, one side is always in reverse bias and the other is forward biased regardless of the applied bias. The ii-layer is a composite intrinsic layer made up of two deposited semiconductors, with the larger bandgap layer closer to the light source. By adjusting the sign and the magnitude of the bias, the depletion region will extend into only a portion of the diode thus collecting only the portion of the spectrum whose absorption dominates at that depth. While the device can operate within a very modest voltage

range (+/−1.0 V), colour separation, especially blue/green colour separation, is poor.

Another two-terminal device created by Böhm *et al.* is a p-i-i-i-n structure (where the dielectric constant of the structure is modulated), in which the depletion depth varies as a function of bias [30, 36]. The response curve maximum shifts continuously from 490 nm to 620 nm, and the sensitivity increases as the reverse bias increases from 0 to 1 V. For small reverse bias, the depletion depth extends from the p-side of the junction (diode topside), which weights the optical response towards the blue. Increasing the bias extends the depletion depth through the diode, thus allowing collection of longer wavelength radiation.

The two-terminal multispectral diode approach has a major disadvantage in that its operation requires that multiple measurements at different bias levels be made sequentially. This means that sensors will be susceptible to temporal artefacts such as image smearing. In addition, to integrate the diodes into the circuit, the control circuitry will have to operate at partitioned voltages requiring novel circuit architectures. The stacked diode approach circumvents this problem.

It is possible to solve the temporal artefact issue by collecting all images simultaneously. If three separate p-i-n diodes are stacked on top of one another and separated by interspersed transparent layers, then it is possible to have three separate sets of circuits (Fig. 7) [24]. Each diode is designed to be selective to only a given wavelength range through a combination of intrinsic layer composition and thickness. The upper diodes collect shorter wavelength light, and simultaneously act as the shorter wavelength filter for the lower diodes. The transparent layer is either a single transparent conductor, or a stack of two transparent conductors separated by a dielectric layer to provide complete electrical isolation. Such an approach, while somewhat more complex to fabricate, produces a sensor that can simultaneously readout all three colours, thus eliminating temporal artefacts caused by changes in illumination or motion. Fabrication costs of the diode stack are partially offset by the removal of colour filter formation steps used for planar diode concepts. In addition, by electrically separating the diodes, the full supply voltage can be applied to each diode, so that standard signal conditioning circuits can be utilised. The stacked diode concept shows excellent colour separation (Fig. 8), especially for the red, which shows superior blue and green rejection. It is comparable to resist-based colour filters currently used. Care will have to be taken to minimise the absorption losses of the shorter wavelength signals, and interference losses for longer wavelength signals.

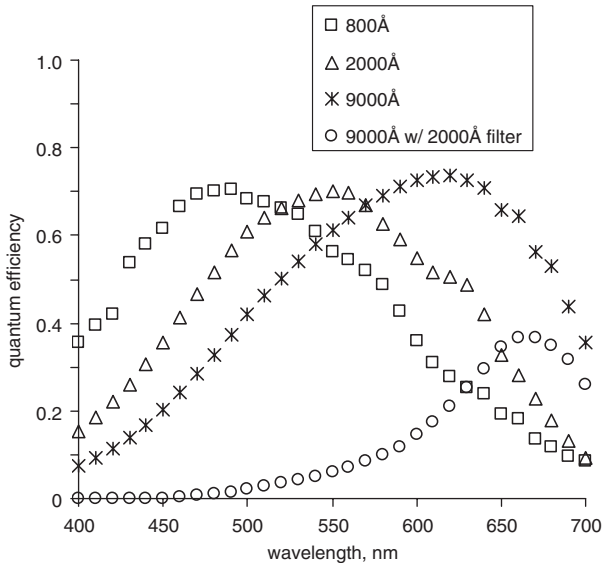


Fig. 8 *Quantum efficiency of a-Si:H diodes of varying i-layer thickness*
The curve labelled 9000 Å w/2000 Å filter, was a 9000 Å diode with a 2000 Å intrinsic a-Si:H layer placed on top of the transparent conductor to demonstrate the effect of stacking diodes on top of one another

2.1.3 Pixel architectures: The photodiode is only an element within the photosensor array pixel. Therefore, it is necessary to understand the operational issues of the pixel circuit. Fortunately, the use of the elevated photodiode allows for advanced pixel circuit concepts to be implemented with good performance, since the circuit area no longer has to be optimised with respect to the photodiode area. Several designs have been implemented using the elevated photodiode concept and are discussed below. However, as the 3T source follower design is the most prevalent, it will be considered first along with the issues that are considered with circuit design, including signal-to-noise ratio and noise components. Then a description of a constant current pixel, and a self-adaptive high dynamic range pixel will be presented. The quality of images collected with two versions of the device are shown in Figs 9 and 10. Both images were collected with VGA pixels, however, Fig. 9 was the first attempt at a sensor, with 6.9 µm pixel on an analogue out chip with a picture collected in a laboratory. Figure 10 shows a field-collected image from a 4.9 µm pixel embedded in a prototype camera with fixed optics. The sharpness of the picture is limited by the optics not the sensor.

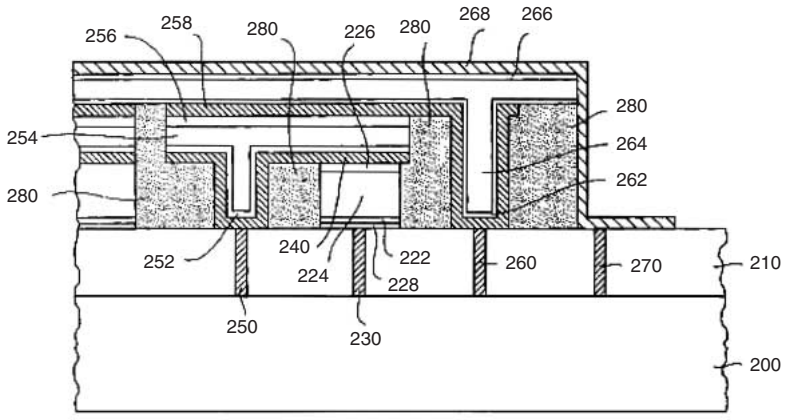


Fig. 7 *Cross-section of a triple-stack diode for collecting three light spectra simultaneously [24]*
Layers 240, 258, and 268 are transparent conductive layers that allow electrical contact to both sides of either diode

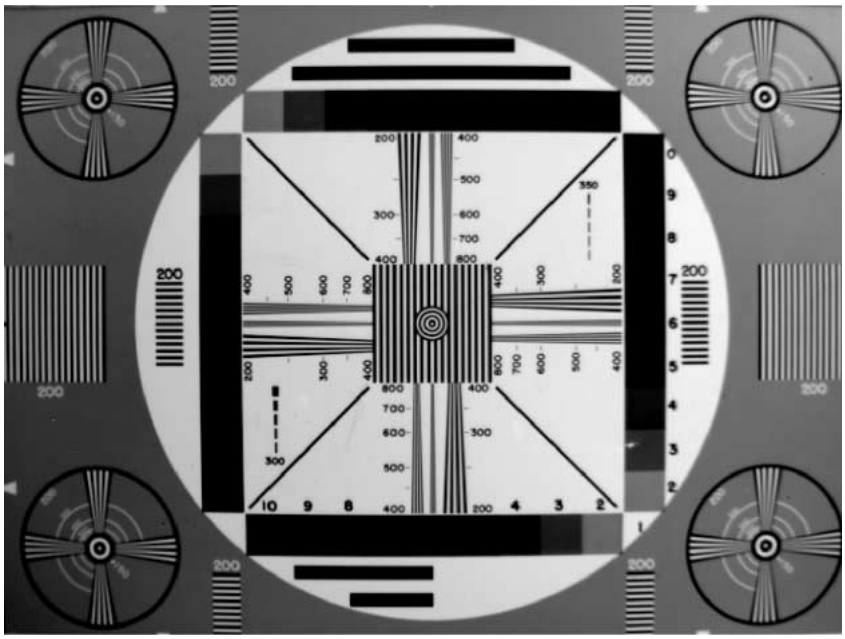


Fig. 9 *Test pattern image taken by a 10-bit VGA (640 × 480) a-Si:H photodiode array, with 5.9 μm by 5.9 μm pixels and 0.35 μm CMOS process*

Fig. 10 *Daylight image of a 4.9 μm × 4.9 μm VGA 640 × 480 pixel integrated camera sensor module*
Average scene illuminance is 1900 lux

The standard 3T pixel design used in the majority of image sensors is the source follower design, the schematic of which is shown in Fig. 11. In this pixel, the reverse-biased diode is connected to ground and the sensing node along with three NMOSFETs [24]. Transistor M1 resets the photodiode to $V_{dd}-V_{tn}$, this defining the start of the integration period, and again after the end of integration to provide a sample reset. When the row line is asserted, M3 enables the source-follower device M2 to buffer the PD voltage onto the column line. An amplifier at the bottom of each column samples the column line at the end the integration period and immediately after sample reset. The column amplifier outputs a signal equal to ($V_{PD\,reset}-V_{PD\,integrated}$), which produces a doubly sampled bias value. This design provides excellent interpixel leakage suppression when used with the patterned pixel definition approach.

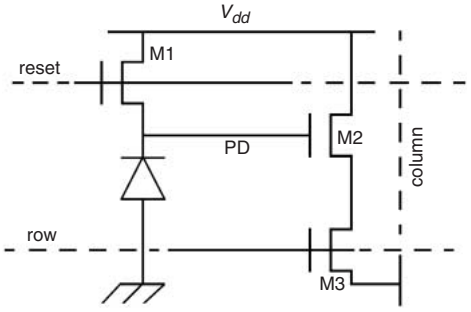


Fig. 11 *3T source follower pixel schematic*

One very interesting scaling feature is that as the pixel size is reduced, sensitivity decreases for pixels with crystalline diode, as the proportion of the diode collection area to the

total pixel must decrease to first order. For elevated photodiode pixels, the sensitivity remains constant as a function of scaling, as long as the light collection area proportion of the pixel remains constant. This remains true as long as the sense node capacitance is dominated by the photodiode junction capacitance. In most designs, the pixel contact layer to the diode extends through most of the pixel >90%, and as long as the local electric field is 5×10^3 V/cm or higher, virtually all of the photogenerated charge is collected [31, 32]. The primary disadvantage to scaling is that decreasing the sense node capacitance increases kT/C noise and pixel reset shot noise.

In pixel operation the noise of the p-i-n diode limits signal quality and helps to set the detection limit of imagers. Blecher *et al.* has published several papers on the topic from diode measurements to 3T pixel analysis, which together form a fairly comprehensive analysis of a-Si:H-based pixel noise [8, 33–35]. There are several noise mechanisms that influence the overall diode noise, including shot and $1/f$ noise for the photo and dark current, as well as parallel resistance thermal noise (kT/R_p). Figure 12*a* shows the magnitude of each of these noise sources as a function of illumination for a 10 μm pixel. $1/f$ noise is logarithmically related to integration times the square of the current. The shot noise is inversely related to integration time and proportional to current. As mentioned above, thermal noise is inversely related to the parallel resistance thermal noise, and mostly consists of thermal carrier generation within the depletion region. It has been found that the dominant noise sources are thermal noise associated with the diode series resistance (kTR_s) and kT/C noise [8]. Both of these noise sources are only proportional to temperature and the design of the diode and pixel elements. The thermal noise of the series resistance is governed by the non-depleted layers of the diode, contact layers, the interfaces between them, and the interconnect structures. kT/C noise is the largest single noise component in the 3T design, and is governed by the total capacitance of the 3T sensing node. For larger pixels the capacitance is primarily due to the diode junction capacitance.

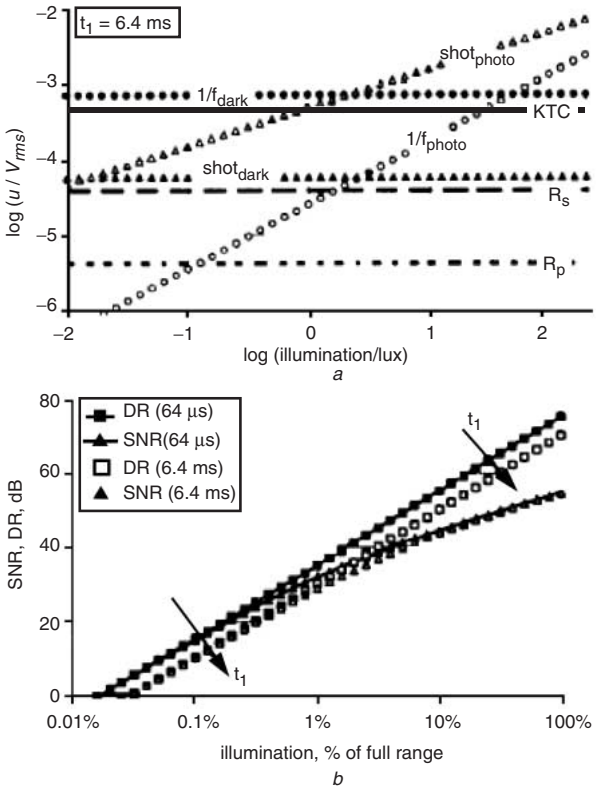


Fig. 12 *Illumination effects on noise*
a Changes in noise sources as a function of illumination for a 3T pixel
b Changes in SNR and DR as a function of relative illumination for two different integration times
Both are for the HIRISE II 3T pixel [8]

There are several approaches that may be employed to minimise contributions of each mechanism. Pixel scaling reduces SNR and DR proportionally with pixel area as long as diode and sense node capacitances scale. As long as the applied field across the diode from a reduced area terminal is strong enough to collect charge from the entire pixel, then the collected signal will not suffer. Indeed, as the sensitivity of the pixel is inversely proportional to the sense node capacitance, then in fact the sensitivity will increase at the same time. If the source follower capacitance can be more than proportionally reduced relative to the diode capacitance, then some SNR improvement can be realised, but in general kT/C noise will increase. Reduction of pixel area will produce reductions in shot and $1/f$ noise. Series resistance thermal noise can be reduced by increasing the RC delay of the of the output line to the signal amplifier [8]. In addition, since thermal noise of the diode series resistance is largely dominated by the p- and n-layer resistances, maximising active dopant concentration and minimising layer thickness will help to lower R_s.

Another series of noise reduction techniques can be performed using collected reference data about pixel behaviour. Since kT/C noise is constant with respect to sampling conditions, it is possible to remove it from the pixel through correlated double sampling (CDS). CDS techniques involve taking a reference measurement prior to collecting the actual sample data, and subtracting it. Since the sample data will contain the same amount of noise as the reference measurement, the noise is removed. This technique involves storing the pre-integration data until sampling is complete, which may be accomplished with a capacitor or a memory element. This is attractive from the viewpoint that it does not require specialised junction engineering, however, system cost rises due to the additional die area required for the capacitor banks or memory elements.

The 3T source follower design requires that the p-i-n junction undergo voltage transients during signal integration and reset, however in certain circumstances, it is desirable to hold the diode voltage constant and monitor the photocurrent. The self-aligned pixel definition technique can suffer from unacceptable interpixel leakage under use conditions. Current mirrors, on the other hand, have very high interpixel leakage current rejection since pixels are held at constant bias. Schneider *et al.* have designed and implemented a current-mirror-based pixel circuit for that purpose (Fig. 13) [36]. The output of the current mirror (M1 through M5) discharges an integration capacitor that is tied to the sense node of a source follower, M7. Their design is an 18 μm × 18 μm pixel in a 0.5 μm CMOS flow, and has a transient response time that is faster than 64 μs. One advantage is that holding the diode at constant bias minimises interpixel leakage, and allows the diode to remain in a steady-state condition for low light conditions. The other advantage of this design is that the sense node capacitance is decoupled from the photodiode, thus allowing some design freedom in setting pixel sensitivity. However, capacitor sizing needs to be balanced against the overall pixel area. The primary disadvantage of the design is the greatly enlarged pixel area relative to a 3T design which would be expected to be 90% smaller using the same process technology.

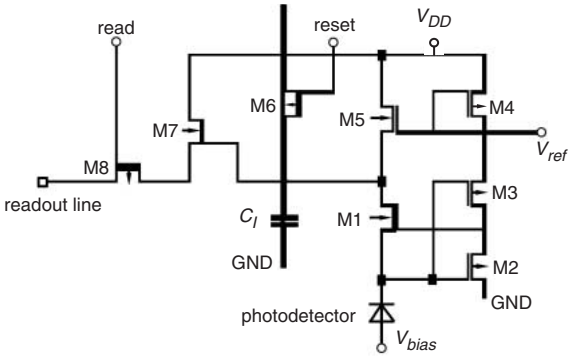


Fig. 13 *Schematic diagram of the constant-voltage pixel circuit [36]*

The primary advantage of the source follower architecture is that it is the most compact design that allows for separate reading and reset function, required for image signal processing. This makes it attractive for high volume applications where cost is a driving factor. Current voltage conversion is performed in the pixel, and it provides excellent buffering for the sense node. However, it is quite limited in providing high dynamic range, or other specialised signal processing functions. One pixel architecture of note is the locally auto-adaptive sensor (LARS) pixel developed by Benthien *et al.* [26]. The LARS pixel architecture is designed to provide large dynamic range (>100 dB, when compared to around 60 dB for source follower-based pixels), with minimal fixed pattern noise, high contrast, and minimal thermal drift. The device uses an integration capacitor, and a comparator to determine how long it takes for the photodiode current to reach a pre-set level. This decay rate is then translated into an a digital intensity to create the image. The highly complex nature of the pixel makes the use of the elevated photodiode concept to maximise the diode light collection capabilities.

2.2 Organic light-emitting devices

Organic light-emitting devices (OLED) have recently created much interest in the flat panel display field because of their potential for high brightness, high power efficiency, and large area fabrication [37]. Since these materials are non-crystalline, they also provide a viable option of integrating a light emission source on silicon [10, 11]. While successful integration has been demonstrated, several significant, but solvable issues remain before they gain commercial acceptance. There are two classes of organic light-emitting materials, polymer-based films (also known as light-emitting polymers (LEP)), which are deposited through solvent-based spin-on methods, and small molecule-based materials (also known as molecular OLEDs) that are typically deposited through sublimation or evaporation. The next Section will discuss OLED technology and will concentrate on the differences between the two forms of OLEDs being commercially pursued. Then a discussion of OLED process flows and integration challenges will be presented, and pixel drive circuitry.

2.2.1 Junction technology: While OLEDs typically consist of a rectifying junction, the carrier transport mechanism is fundamentally different between OLED and compound semiconductor LEDs. On the anode side there is a hole-emitting contact layer (usually indium-tin oxide (~100 nm), ITO, or polyalanine; typically a conductive high work-function material), a hole transport layer (HTL) (such as α-naphtylphenylbiphenyl diamine) (20–50 nm), a light emission layer (~20–40 nm) (EML), an electron transport layer (~30 nm) (ETL), and finally a cathode contact layer (a conductive low work-function material) (~10 nm) made out of a variety of alkali and alkaline-earth-based films and alloys [37]. In some designs the EML and ETL are the same layer, and the entire organic film stack is on the order of 100 nm.

The organic layers are generally neither n- nor p-type, but rather they preferentially conduct a particular carrier due to an asymmetry in carrier mobilities. Mobilities typically are between 10^{-6} and 10^{-3} cm^2/Vs for holes, and 10^{-8} and 10^{-6} cm^2/Vs for electrons, thus requiring that the layers be thin in order for the device to operate [38]. Therefore, the current in the layers is ultimately limited by space charge effects. Injected charges driven by an externally applied voltage into the ETL/HTL interface region form excitons which are the basis for light generation. The exciton will be confined in the material with the lowest exciton energy, but free to migrate within that layer [39, 40]. The exciton diffuses randomly through the matrix until it decays, either radiatively or non-radiatively. The emission from the OLED comes from the same excitonic state that would be formed by photoexcitation. Direct carrier recombination of singlet excitons can generate the photon directly [38].

The richness of organic chemistry allows the fabrication of new materials with different emission properties. LEPs have been developed that emit across the visible spectrum, with low applied voltages (<5 V) and the intensity of light is proportional to current. For both types of OLEDs, the luminescent efficiencies are approaching that of fluorescent light bulbs 20–50 lm/W [39]. OLEDs have been developed to emit from the infrared into the UV using various techniques including complexes of rare-earth elements into small molecules, designing the bandgap of polymers, and inserting optical dyes into light-emitter layers [39, 41–43]. Typically, the electroluminescent efficiency of the molecular OLED material itself is <1%. To increase the efficiency of these layers, a matrix of an organic conductor is 'doped' with a low concentration of an efficient radiative recombination material. By use of chelated transition-metal atoms in the molecule, the more common triplet exciton may be used. These approaches can improve the device photon generation quantum efficiency towards 20% [44, 45]. In the case of LEP-based devices, the conduction and photogeneration mechanisms are the same, but the engineering of the various components is done through modification of the polymer during its creation.

For OLED applications, other than for illumination, it is important that the switching transients be controllable. Pinner *et al.*, developed a phenomenological model that describes the excitation and decay transients for LEP devices [46]. They used the same transport model for inorganic semiconductors, but modified the mobility definition to account for field-induced effects. They show that the OLED devices have a characteristic delay between pulse application and light emission, and that this is a universal characteristic of LEP and molecular OLED materials [46–48]. This delay time is a function of the time it takes for injected holes and electrons to come together near the cathode, and is limited by the very low mobilities. It is expected that the recombination region is nearer the cathode due to the much lower electron mobility with respect to holes. The time scale is on the order of 10^{-7} s, but is expected to be controlled by layer thickness and local field effects. The decay time consists of two processes, an extremely fast decay less than 10 ns, and a slower decay based on the exciton decay time [46]. The implication is that it should be possible to build devices with at least a 10 MHz bandwidth given current technology.

2.2.2 Structure and process technology: All OLED materials pose significant but surmountable integration challenges, including moisture and oxygen sensitivity, processing temperature, and patterning techniques. As most cathode materials are alloys containing alkali and alkali-earth elements, the devices must be moisture isolated. Typically this is accomplished by encapsulating the stack in a moisture barrier, however, processing between the time the cathode is deposited until the encapsulant is in place requires extra care [11]. Both molecular OLED and LEP materials are oxygen sensitive, so care must be taken to minimise air exposure until they are encapsulated. LEP material also is limited to processing temperatures below 120°C, which constrains all post-deposition steps. Fortunately for molecular OLEDS, their sublimation temperature ranges from 300–450°C [49], thus rendering them less susceptible to temperature constraints.

A fundamental processing problem is OLED patterning. In most applications, there is a need to have full colour imaging, which requires spatial distribution of at least three separate colours. This can be accomplished either through the use of different colour emitting OLED, or by the use of traditional colour filter technologies. While colour filter process flows can rely upon a barrier layer to protect the OLED during resist patterning and stripping, the result is an array that must generate more intense light to achieve the equivalent brightness to a non-filtered array. Therefore, it would be preferable to develop a technique to deposit a mosaic of coloured OLEDs. As the conventional photoresist removal processes involve the use of oxygen-rich plasma ashing or aqueous-based resist stripping baths, there are obvious problems with protecting the already deposited diode. It is possible to protect each diode sub-array with a contact and passivation layer, but this requires additional processing, and will limit the minimum pixel size. On the other hand, if diode passivation and a dry etch technique is developed, then it is also possible to build stacked diodes to achieve full colour at each pixel. What is not known is the effect of light absorption of upper diodes from lower diode emission. The pixel size of 12 μm used by Abraham *et al.*, should permit stacking [10]. Therefore for LEP spin-on materials, the colour filter technique seems like the most likely one to succeed in the near-term. The molecular OLED technologies can utilise direct writing techniques such as shadow mask deposition or inkjet writing [50, 51]. Non-writing integration flows could rely on contact layer hardmasking, however, damage to the periphery of the OLED will need to be considered to avoid degradation of electrical properties through shorting.

2.2.3 Pixel architecture: Microdisplay OLED pixels are driven by pulse-width modulation. The operation of the in-pixel pulse-width modulation circuit is shown in Fig. 14 where time-multiplexed RGB analogue data are input at DATA_IN [10]. The pixel uses PMOS transistors instead of capacitors for data-value storage. The drive signal to the diode is generated with a simple two-stage, PMOS input comparator, which produces a total bias current of 8 nA. In this example, the complete circuit occupies the area under a 12 μm × 12 μm pixel in the 0.35 μm CMOS process. The data is sampled and held through the SET1/SET2 switches. VRAMP is a ramp voltage that is reset every half- display period and spans the analogue voltage range. Inputs PATH1/PATH2 and SWITCH are used along with VRAMP and the voltage on DATA1/DATA2 to set the pixel output voltage, OUT, at V_{dd} for a time-width proportional to the input level, DATA_IN. Since a time average of zero is not needed for a LEP display, a unique VRAMP shape can be used to provide a 100% display duty cycle. In addition gamma correction can be provided by modifying the shape of VRAMP. Operation of a completed display is shown in Fig. 15. One design challenge is accommodation of OLED operational voltages. LEP materials typically operate at less than 5 V, which makes them compatible with some current submicron CMOS processes. While molecular OLEDs also work at relatively low voltages, <10 V, however, this is still higher than CMOS processes with <1 μm channel length. Dual-gate processes are one way to work around the issue, but will raise overall process costs. Re-engineering the FETs is required to utilise these materials, but this is a solvable issue. For example dual gate processes can be created to provide low voltage high speed operation for the mixed signal portion of the circuit, and higher-voltage devices would be created to drive the pixels. Of course the process requires additional masks and implant schemes thus increasing process cost to some degree. Since light output is proportional to applied bias, for both materials it will be important for the device efficiency to match the application requirements.

3 Elevated diode applications

There are three rationales for implementing elevated diode array structures in CMOS devices: (i) a desire to maximise light collection or emission for pixel designs that would normally be too cumbersome impossible by other means; (ii) a need to minimise pixel size for optics or cost constraints; and (iii) a need to minimise system costs by

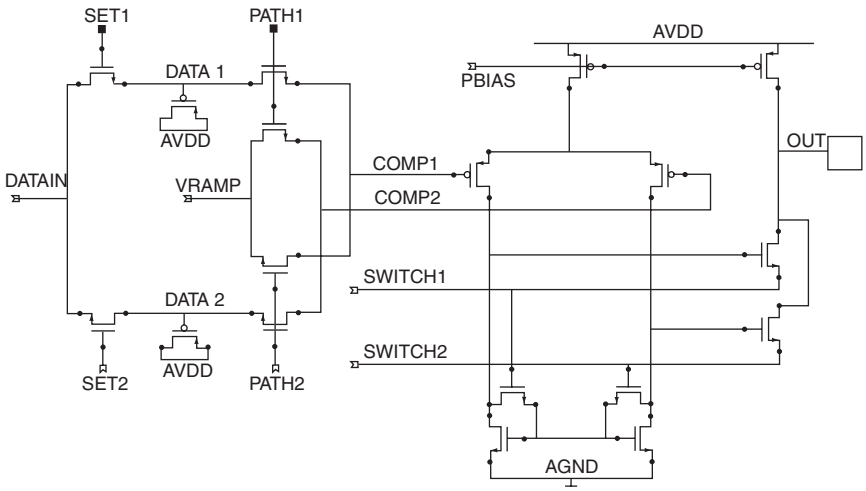
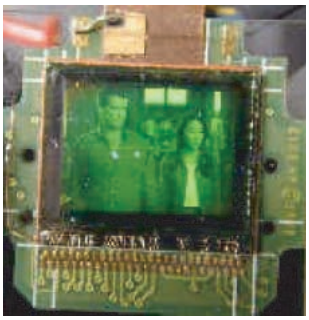


Fig. 14 *In-pixel analogue PMW FET-level schematic*

a



b

Fig. 15
a DVD-generated image displayed on an SXGA microdisplay with 12 μm × 12 μm pixels in a 0.35 μm CMOS process using light-emitting polymers, produced by Agilent Technologies
b Image of the entire OLED display (used by permission)

integration of most system components. Therefore, depending on the exact need of an application, elevated photodiode array-based sensors can be used for any application in which crystalline silicon arrays can be used, and a few where they cannot. For light emission applications, there are no alternatives to OLED-based systems.

For elevated photodiodes there are two additional reasons for implementing them, applications where it is critical to collect all spectral and spatial information from an image, and applications that require a different spectral response from that achievable with crystalline silicon. The elevated photodiode discussion will briefly survey most image sensing applications, then concentrate on a few applications where there is a distinct advantage or no other alternative to employ elevated photodiode arrays. The concept of CMOS-based image sensors has been around since the 1960s [52], but due to poor device performance and large pixel size, the concept lay largely dormant until 1993 [53, 54]. Since then sensors have been employed in the digital still camera market where image quality is the most important criterion, for example the Canon D30 sensor product. However, given the supply voltage for most CMOS applications, the signal quality does not match that of CCDs, so only when power consumption is the key driver and supply voltages drop below 5 V, are CMOS sensors able to outperform CCD devices. This market segment is dominated by portable devices which run on batteries. Therefore, the sensor modules must have low power consumption (<45 mW), operate around 3.3 V, and have as small form factor as possible (8 mm × 8 mm × 5 mm) including the optics.

Across the spectrum of CMOS imager products there are uses for elevated photodiode array-based imagers. At the high end, improved dynamic range and SNR can be realised by a high degree of pixel-level functionality [55]. When integrating the entire signal chain on-chip, noise sources such as power supply, vibration, and pick-up noise sources can be minimised. Fowler demonstrated pixel-level A/D in utilising a bit-serial successive approximation method [56, 57]. In this pixel, they used a CMOS comparator latch structure for the conversion. This requires 12 FETs and 4 diodes control the FETs, but as they shared each comparator among four pixels, the count only averaged 4 FETs/pixel. However, since sequential operation is required to read all pixels, the design is susceptible to motion artefacts unless the clock frequency is very high. Therefore, to minimise the array size and maximise light collection area, pinned photodiodes can be employed. In the high dynamic range architecture of the LARS pixel, the elevated photodiode concept is required. Since the pixel has 24 transistors, large linear capacitors, and other components, it will remain well above a 12 μm × 12 μm pixel size. It is designed for critical imaging applications such as automotive collision avoidance where the ability to detect

detail is critical. Therefore, it must have significant photodiode area coverage to avoid loss of spatial information.

In the typical 3T design in which pixel size minimisation is the most important consideration, optimal sensitivity is achieved in crystalline silicon photodiodes that cover about 50% of the pixel. Scaling of the pixel to finer line geometries allows for simple pixel side reduction, but at a significant cost. As the minimum gate length is reduced, channel leakage increase, so care must be taken to minimise this effect. Scaling reduces the supply voltage, which reduces the usable voltage swing for A/D. Also, more levels of interconnect are required to satisfy routing requirements outside of the pixel and sometimes within it. As more interconnect layers are employed, the thicker the dielectric stack becomes, the higher the degree of telecentricity of the sensor. This reduces the pixel light acceptance angle, thus requiring more expensive optics to compensate. Microlensing can be used, but is a less effective solution as the distance between the lens and the diode grows. Elevated photodiodes on the other hand do not suffer from these issues. The proportion of the pixel area covered by the photodiode remains constant, thus relaxing constraints on gate length scaling and various optical optimisation issues such as light collection area. The sensing element is on top of the interconnect so that the acceptance angle remains large.

Photodiode arrays are now the technology of choice for electronic navigation input devices such as mice and trackballs for personal computers [11]. These devices employ small diode arrays typically 64×64 pixels that operate at very high frame rates $\sim$1000 to 2000 frames per second to detect motion. In these sensors, a motion algorithm is employed outside of the array to determine motion. Another navigation device that has been proposed is one in which a system displays a virtual keypad, and monitors images of fingers touching portions of the keypad to symbolise key presses. It best operates by detecting position and motion at a non-visible wavelength, though alignment between the keypad and the sensing signal would be required. The sensor requirements would be high enough resolution to detect the normal range of motion, a moderately high frame rate, and sensitivity to at least two wavelengths, most likely in the near infrared. Since the current market for such devices would be portable systems that are too small for their own keypad, it is natural to assume that a camera with a small form factor and low power consumption is required. Therefore there is a premium for small pixel size to enhance sensor resolution. Therefore, such a device would benefit from elevated photodiode arrays. If a-Si:H, it could be Ge-doped to improve infrared sensitivity.

Arrays are ideal for parallel processing or testing, and there are a couple of possible parallel sensing systems for chemical applications. Narrow-band spectrometers can be made by adjusting the intrinsic layer bandgap to achieve the desired optical range from the UV to the near IR. The array could be a linear or low row number array. Then depositing a variable thickness interference filter over the diode array in the column direction, one can make narrow band high spectral resolution spectrometers with parallel readout. Performing differential analysis on the data output, it would be possible to device extremely high resolution in such detectors. For parallel chemical testing photodiode arrays can also serve as a disposable test bench, such as DNA fragment analysis for genomics. One system would incorporate sample placement, detection and analysis on one device. Chemical target elements can be pre-spotted directly over the photodiode to maximise light collection (about 50%) and simultaneously eliminate the optics. The detection mechanism could be based upon optical fluorescence, cathodoluminescence, electroluminescence, or absorption [47]. Currently systems that perform this analysis are large optical benches using an off-board CCD array for parallel readout, or a photomultiplier tube (PMT) or avalanche photodiode (APD) and a focused light source for serial readout. However, given the ability to produce low-noise detection schemes at pixel level, and the close proximity of the weakly emitting source to the sample, it should be possible to create a low-cost high performance detector. By using the elevated photodiode concept, it will be possible to keep costs of these units down.

Microdisplays are devices that can produce an image for viewing from a very small array, typically a few millimetres across [11]. OLED microdisplays have several advantages over LCD-based displays, lower power operation, and wide viewing angle [10]. Even though OLED devices consume more power than an LCD device, any LCD-based system that utilises an illumination source will consume more power than an OLED-based system, since the LCD illuminator source must accommodate peak, not average brightness. Given that OLED technology appears to have the ability to ultimately produce more efficient junctions than III–V based LEDs, the OLED power efficiency edge will improve further. Liquid crystal displays tend to have a very limited viewing angle, which is not an issue for emissive displays like OLED-based systems. Additionally, LCD-based systems create colour frame-sequential timing of RGB sources, which can lead to colour separation caused by rapid eye movement. OLED concepts can employ color filters, thus eliminating such artefacts. Many applications have been proposed for such displays, including a two-display lightweight headset for entertainment or medical imagers; and a monocular versions for wearable computers, data displays for confined spaces or military viewfinders, or be used as viewfinders in digital cameras or medical imagers [11].

Since conceptually it is quite simple to integrate OLED devices onto integrated circuits, a natural application of them is for use as the light-generating element in emissive microdisplays. OLEDs are efficient Lambertian emitters that operate at voltage levels (3–10 V), and are capable of luminance greater than 100 000 cd/m^2, even though for most applications lower luminance would be sufficient. Luminance is proportional to current, so gray scale is easily controlled by a current-control pixel circuit. Their response times are much shorter than for liquid crystals, an important feature for video displays. In a few instances both LEP and molecular OLEDs have been integrated into standard CMOS circuits to produce microdisplays. Abraham *et al.* demonstrated an XGA monochrome device (1024×768 pixels) that achieves 200 Cd/m^2 brightness at low power ($<$50 mW) with fast 1 µs response times [10]. More recently, Howard and Prache described an SXGA monochrome device (1280×1024 pixels) using a 12 µm pitch [11]. In both instances, the devices presented appear to be ready for commercialisation. The eMagin corporation has developed microdisplay technology for head-up applications [11]. The pixel driver circuit differs from an LCD driver circuit in that it must provide a constant current to the OLED device, and must be controllable over a range at least 100:1 in order to allow for high-contrast images. A typical display should have a white luminance similar to CRT monitors of about 150 cd/m^2, which would require 20 nA to drive a single 15 µm $\times$ 15 µm pixel. For an SVGA microdisplay, this multiplies to the quite modest value of

29 mA for an SVGA active matrix. The second most important component of an active-matrix OLED display is the bias storage element. This is typically accomplished using a capacitor as the memory element.

One application that highlights the use of both the input and output devices utilising elevated diode technology is a fully functional SXGA camera that is only $\sim 2\,\text{cm} \times 2\,\text{cm} \times 7\,\text{mm}$. Both an elevated photodiode imager with integrated optics and an OLED-based microdisplay could be placed adjacent to one another in a package that includes image processing, memory, a battery, and a cable connection. The 7 mm thickness constraint would be for the integrated optics to allow for imaging and viewing. The limiting element in this case will be the user interface.

4 Summary

Elevated diodes allow integration of novel materials to create new unique devices such as ultra-small image sensor arrays and low-power microdisplays. They provide unique capabilities including: (i) the ability to separate photodiode from of other pixel circuit elements; (ii) the ability to maximise light collection area; (iii) the ability to engineer semiconductor properties to precisely tailor spectral response; (iv) the ability to create multijunction or multiple diode layers; and (v) the ability to place efficient light-emitting structures onto silicon-based integrated circuits. Early imager arrays have already performed at least as well as current crystalline silicon counterparts with pixels that are twice as large. Using the elevated photodiode concept it has been demonstrated that it is indeed possible to utilise very advanced pixel circuit concepts that require high transistor counts without sacrificing sensitivity. Furthermore, by utilising the advanced process capabilities of an integrated circuit manufacturing environment, it is possible to produce lower cost sensors of equivalent or better performance for smaller pixel sizes using elevated photodiodes. On the other hand, the elevated diode concept is the only way to achieve an emissive microdisplay with modest operating voltages. Emissive microdisplays achieve higher contrast and lower power consumption than LCD-based systems.

It is clear that products utilising the elevated diode concept are the first class of monolithic instrument to be successfully fabricated. It demonstrates that the maturity of the semiconductor industry has reached the point where the monolithic integration of new physical structures onto integrated circuits is becoming economical for high-volume manufacturing. It will continue as ever more intriguing devices are created ushering in the third generation of semiconductor devices, monolithic instruments, and a new application based on this higher degree of miniaturisation.

5 References

1 Schaufelbuhl, A., Schneeberger, N., Munch, U., and Waelt, M. *et al.*: 'Uncooled low-cost thermal imager based on micromachined CMOS integrated sensor array', *Microelectromech. Syst.*, 2000, **10**, (4), pp. 503–510

2 Abshire, P., and Andreou, A.G.: 'Capacity and energy cost of information in biological and silicon photoreceptors', *Proc. IEEE*, 2001, **89**, (7), pp. 1052–1064

3 Blalock, T.N., Baumgartner, R.A., and Hornak, T.: 'A 1.5 GOPS analog CMOS array processor with integrated optical image acquisition for position encoding applications'. Symposium on VLSI Circuits, Digest of Technical Papers., 1998, pp. 204–205

4 Yadid-Pecht, O., Ginosar, R., and Shacham Diamand, Y.: 'A random access photodiode array for intelligent image capture', *IEEE Trans. Electron Devices*, 1991, **38**, (8), pp. 1772–1780

5 Renshaw, D., Denyer, P.B., Wang, G., and Lu, M.: 'ASIC vision'. Proc. IEEE Custom Integrated Circuits Conference, Baston, MA, USA, 1990, pp. 7.3/1–4

6 Theil, J.A., Cao, M., Kooi, G., Ray, G.W., Greene, W., Lin, J., Budrys, A.J., Yoon, U., Ma, S., and Stork, H.: 'Hydrogenated amorphous silicon photodiode technology for advanced CMOS active pixel sensor imagers', *Mater. Res. Soc. Symp. Proc.*, 2000, **609**, pp. A14.3.1–A14.3.6

7 Theil, J.A., Haddad, H., Snyder, R., Zelman, M., Hula, D., and Lindahl, K.: 'Performance of a-Si:H photodiode technology-based advanced CMOS active pixel sensor imagers', *Proc. SPIE-Int. Soc. Opt. Eng.*, 2001, **4435**, pp. 206–213

8 Blecher, F., Schneider, B., Sterzel, J., Hillebrand, M., Benthien, S., and Böhm, M.: 'Noise analysis of imagers with a-Si:H pin diode pixels', *J. Non-Cryst. Solids*, 2000, **266**, pp. 1188–1192

9 Harada, N.: 'Amorphous semiconductor technologies and devices' Vol. 6 (North Holland, 1984), p. 283

10 Abraham, H.E., Antoniadis, H., Roitman, D.B., Frischknecht, K., Blalock, T.N., Kishimura, K.A., Knotts, T.A., Theil, J.A., Bright, C., Miller, J.N., and Moon, R.: 'XGA resolution full video microdisplay using light emitting polymers on a silicon active matrix circuit', *Proc. SPIE-Int. Soc. Opt. Eng.*, 2001, **4105**, pp. 37–52

11 Howard, W.E., and Prache, O.F.: 'Microdisplays based upon organic light-emitting diodes', *IBM J. Res. Dev.*, 2001, **45**, (1), pp. 115–127

12 Prache, O.: Digest of Soc. Information Display Conf., 2001, p. 514

13 Fischer, H., Schulte, J., Giehl, J., Böhm, M., and Schmitt, J.P.M.: 'Thin film on ASIC-a novel concept for intelligent image sensors', *Mater. Res. Soc. Symp. Proc.*, 1992, **285**, pp. 1139–1144

14 Theil, J., Lefforge, D., Kooi, G., Cao, M., and Ray, G.: 'Mid-gap states measurements of low-level boron-doped a-Si:H films', *J. Non-Cryst. Solids*, 2000, **266**, pp. 569–573

15 Fischer, H., Schulte, J., Rieve, P., and Böhm, M.: 'Technology and performance of TFA (thin film on ASIC)-sensors', *Mater. Res. Soc. Symp. Proc.*, 1994, **336**, pp. 867–872

16 Theil, J.A., Snyder, R., Hula, D., Lindahl, K., Haddad, H., and Roland, J.: 'a-Si:H photodiode technology for advanced CMOS active pixel sensor imagers', *J. Non-cryst. Solids*, 2002, **299**, pp. 1234–1239

17 Zhu, Q., Lule, T., Stiebig, H., Martin, T., Giehl, J., Zhou, J., Fischer, H., and Böhm, M.: 'Color array in TFA technology'. Proc. 4th Int. Conf. on Solid-state and integrated circuit technology, 1995, pp. 727–729

18 Morrison, S., Servati, P., Vygranenko, Y., Nathan, A., and Madan, A.: 'Reduction of dark current under reverse bias in a-Si:H p-i-n photodetectors', *Mater. Res. Soc. Symp. Proc.*, 2002, **715**, pp. 701–706

19 Street, R.A.: 'Hydrogenated amorphous silicon' (Cambridge University Press, Cambridge, UK, 1991), pp. 370–371

20 Street, R.A.: 'Thermal generation currents in hydrogenated amorphous silicon p-i-n structures', *Appl. Phys. Lett.*, 1990, **57**, (13), pp. 1334–1336

21 Theil, J.A., Kooi, G., and Varghese, R.: 'High deposition rate hydrogenated amorphous silicon (Method, material, and apparatus)'. US6436488, EP1164206, JP2002047568A, 2001

22 Matsuda, A.: 'Plasma and surface reactions for obtaining low defect density amorphous silicon at high growth rates', *J. Vac. Sci. Technol. A, Vac. Surf. Films*, 1998, **16**, (1), pp. 365–368

23 Theil, J.A., Ray, G., Perner, F., and Cao, M.: 'An improved interlayer dielectric for passivation of an elevated integrated circuit sensor structure'. US6051867, EP1052698, JP2001024059, 2000

24 Theil, J.A., and Ma, S.: 'A stacked multiple photosensor structure including independent electrical connections to each photosensor'. US6373117, EP1050907, JP2001007310, 2002

25 Eckhardt, A., Schneider, B., Blecher, F., Sterzel, J., Seibel, K., and Bohm, M. *et al.*: 'Image sensors in TFA technology and their applications for image pre-processing'. Proc. ESSDERC, 1998, pp. 208–211

26 Benthien, S., Lule, T., Schneider, B., and Wagner, M. *et al.*: 'Vertically integrated sensors for advanced imaging applications', *IEEE J. Solid-State Circuits*, 2000, **35**, (7), pp. 939–945

27 Mutze, F., Seibel, K., Schneider, B., Hillebrand, M., Blecher, F., Lule, T., Keller, H., Rieve, P., Wagner, M., and Böhm, M.: 'UV imager in TFA technology', *Mater. Res. Soc. Symp. Proc.*, 1999, **557**, pp. 815–820

28 Schroten, E., Zeman, M., van Swaaij, R.A.C.M.M., Vosteen, L.L.A., and Metselaar, J.W.: 'Simulation of hydrogenated amorphous silicon germanium alloys for bandgap grading', *Mater. Res. Soc. Symp. Proc.*, 1999, **557**, pp. 773–778

29 Knipp, D., Stiebig, H., and Wagner, H.: 'Stabilized three color piinip sensor for high illumination conditions', *Mater. Res. Soc. Symp. Proc.*, 1998, **507**, pp. 225–230

30 Böhm, M., Blecher, F., Eckhardt, A., and Seibel, K. *et al.*: 'Image sensors in TFA technology-status and future trends', *Mater. Res. Soc. Symp. Proc.*, 1998, **507**, pp. 327–338

31 Lule, T., Benthien, S., Keller, H., Mutze, F., Rieve, P., Seibel, K., Sommer, M., and Böhm, M.: 'Sensitivity of CMOS based imagers and scaling perspectives', *IEEE Trans. Electron Devices*, 2000, **47**, (11), pp. 2110–2122

32 Rieve, P.: 'Spektralselektive optoelectronische sensoren auf der basis amorphen siliziums'. PhD thesis, Univ.-GH Siegen, Germany 2000

33 Blecher, F., Seibel, K., and Böhm, M.: 'Photo- and dark current noise in a-Si:H pin diodes at forward and reverse bias', *Mater. Res. Soc. Symp. Proc.*, 1998, **507**, pp. 175–180

34 Blecher, F., Schneider, B., Hillebrand, M., and Böhm, M.: *Mater. Res. Soc. Symp. Proc.*, 1999, **557**

35 Blecher, F., Seibel, K., Hillebrand, M., and Böhm, M.: 'New method to determine the a-Si:H pin diode series resistance by noise measurements', *Mater. Res. Soc. Symp. Proc.*, 1998, **507**, pp. 169–174

36 Schneider, B., Blecher, F., Eckhardt, A., and Seibel, K. *et al.*: Proc. OPTO 98, **233**, 1998
37 Forrest, S.R.: 'Active optoelectronics using thin-film organic semiconductors', *IEEE J. Sel. Top. Quantum Electron.*, 2000, **6**, (6), pp. 1072–1083
38 Ruhstaller, B., Carter, S.A., Barth, S., and Riel, H. *et al.*: 'Transient and steady-state behavior of space charges in multilayer organic light-emitting diodes', *J. Appl. Phys.*, 2001, **89**, (8), pp. 4575–4586
39 Burroughes, J.H.: Presented at the 9th Int. Workshop on Inorganic and organic electroluminescence, Bend, OR, USA, 1998
40 Pope, M., and Swenberg, C.E.: 'Electronic processes in organic crystals' (Clarendon, Oxford, UK, 1982)
41 Khreis, O.M., Curry, R.J., Somerton, M., and Gillin, W.P.: 'Infrared organic light emitting diodes using neodymium tris-(8-hydroxyquinoline)', *J. Appl. Phys.*, 2000, **88**, (2), pp. 777–780
42 Seguy, I., Jolinat, P., Destruel, P., and Farenc, J. *et al.*: 'Red organic light emitting device made from triphenylene hexaester and perylene tetraester', *J. Appl. Phys.*, 2001, **89**, (10), pp. 5442–5448
43 Shoustikov, A.A., You, Y., and Thompson, M.E.: 'Electroluminescence color tuning by dye doping in organic light-emitting diodes', *IEEE J. Sel. Top. Quantum. Electron.*, 1998, **4**, (1), pp. 3–13
44 Baldo, M.A., O'Brien, D.F., You, Y., Shoustikov, A., Sibley, S., Thompson, M.E., and Forrest, S.R.: 'Highly efficient phosphorescent emission from organic electroluminescent devices', *Nature*, 1998, **395**, pp. 151–154
45 Baldo, M.A., Lemansky, S., Burrows, P.E., Thompson, M.E., and Forrest, S.R.: 'Very high-efficiency green organic light-emitting devices based on electrophosphorescence', *Appl. Phys. Lett.*, 1999, **76**, (1), pp. 4–6
46 Pinner, D.J., Friend, R.H., and Tessler, N.: 'Transient electroluminescence of polymer light emitting diodes using electrical pulses', *J. Appl. Phys.*, 1999, **86**, (9), pp. 5116–5130
47 Kovac, J., Wong, T.C., Fung, M.K., and Liu, M.W. *et al.*: 'Transient electroluminescence of single and multilayer organic light emitting devices', *Mater. Sci. Eng. B, Solid-State Mater. Adv. Technol.*, 2001, **85**, pp. 172–176
48 Pinner, D.J., Friend, R.H., and Tessler, N.: 'Analysis of the turn-off dynamics in polymer light-emitting diodes', *Appl. Phys. Lett.*, 2000, **76**, (9), pp. 1137–1139
49 Kowalsky, W., Becker, E., Benstem, T., and Dobbertin, T. *et al.*: 'OLED matrix displays: technology and fundamentals'. Proc. IEEE Int. Conf. on Polymers and adhesives in microelectronics and photonics, 2001, pp. 20–28
50 Meyer, W.: 'Micro dispensing of adhesives and other polymers'. Proc. 1st Int IEEE Conf. on Polymers and adhesives in microelectronics and photonics, 2001, pp. 35–39
51 Mathine, D.L., Jabbour, G.E., Morrell, G.E., and Shaheen, M.M. *et al.*: 'Fabrication of micropixel arrays of bright organic electroluminescent devices'. Technical Digest of CLEO 1998, Lasers and electro-optics, 1998, p. 7
52 Fossum, E., and Krymski, A.: 'High speed CMOS imaging'. Digest of the LEOS Summer Topical Meetings, 2000, pp. I3–I4
53 Fossum, E.R.: 'Active-pixel sensors challenge CCDs', *Laser Focus World*, 1993, **29**, (6), pp. 83–87
54 Mendis, S., Kemeny, S.E., and Fossum, E.R.: 'CMOS active pixel image sensor', *IEEE Trans. Electron. Devices*, 1994, **41**, (3), pp. 452–453
55 Pain, B., and Fossum, E.R.: 'Approaches and analysis for on-focal-plane analog-to-digital conversion', *Proc. SPIE-Int. Soc. Opt. Eng.*, 1994, **2226**, pp. 208–218
56 Yang, D.X.D., Fowler, B., and El Gamal, A.: 'A Nyquist-rate pixel-level ADC for CMOS image sensors', *IEEE J. Solid-State Circuits*, 1999, **34**, (3), pp. 348–356
57 Yang, D.X.D., El Gamal, A., Fowler, B., and Hui, T.: 'A 640×512 CMOS image sensor with ultrawide dynamic floating-point pixel-level ADC'. Tech. Digest of Int. Solid-State Circuits Conf., 1999, p. 308