REDUCTION OF RESIDUAL TRANSIENT PHOTOCURRENTS IN A SI:H ELEVATED PHOTODIODE ARRAY BASED CMOS IMAGE SENSORS

Jeremy A. Theil*

Agilent Technologies, Santa Clara, CA, 95051, U.S.A.
*current contact information: Lumileds Lighting, LLC, MS 91UJ
370 W. Trimble Rd., San Jose, CA 95131, U.S.A., e-mail: jeremy.theil@lumileds.com

ABSTRACT

While a-Si:H based elevated photodiode arrays hold the promise of superior performance and lower cost CMOS-based image sensors relative to those based upon crystalline silicon photodiodes, the one area where a-Si:H based sensor performance has not been as good is in image lag. This problem is only exacerbated by Staebler Wronski Effect induced junction degradation. Image lag is caused by residual charge from photocurrents trapped within the junction once the light source is removed and can be measured for several seconds, even under continuous applied reverse bias. It is seen both in constant and variable bias pixel architectures. However, by carefully controlling a-Si:H junction bias conditions, it is possible to significantly reduce these transient photocurrents. This article will describe how the photocurrent decay time exponent can be reduce by almost an order of magnitude. Finally the physical causes behind image lag in a-Si:H based photodiode arrays will be discussed.

1 INTRODUCTION

Over the last ten years, there has been increasing interest in the use of a-Si:H in photodiode arrays that are monolithically integrated onto integrated circuits [1-3]. Such integration allows a combination of 1) reduced imaging pixel area, 2) reduced sensor cost, 3) lower photodiode leakage, and 4) improved pixel sensitivity. As pixel-level complexity (hence area) grows, the advantages become more apparent. The one area where a-Si:H diode-based pixel performance tends to be deficient with respect to all-crystalline silicon pixels is in image lag. Image lag is typified as a persistent afterimage artifact in the array as a result of charge generated by an earlier measurement (hence the transient photocurrent). There are many systemic causes of image lag in all image sensor technologies, but the high trap-state density of a-Si:H provides an additional mechanism through prolonged carrier emission. In addition, since most a-Si:H diode array architectures use a continuous i-layer to maximize the light gathering area of the array, the junction construction itself may contribute. Therefore we created a novel parametric test structure to try to elucidate various potential mechanisms in a realistic array. The motivation behind this work is to start to identify the causes of this transient photocurrent and how see if there are ways to mitigate it.

2 EXPERIMENTAL

Details of diode fabrication have been presented elsewhere, the resulting structure is pictured in Figure 1a [1,2,4]. All test structures are bounded by a ring diode that is held at the same bias as the measurement structure itself to eliminate injected edge currents. The test structure used in this experiment is a two-channel 2-D interpenetrating diode array consisting of junction area about 8.84×10^5 μm^2 with 940 μm. Such an array mimics layouts for high-density a-Si:H arrays, along with the ability to study the current flow between individual pixels and junctions by aggregating them into larger structures. The n-layer electrode is patterned in a series of 4 μm

square pixels with a 5 μm pitch, in a 188 x 188 array, (see Figure 1b). The two channels each contain 17672 pixels and allow for independent biasing to study interpixel effects. The i-layer thickness was 5500Å, the 200Å thick p-layer boron atomic concentration was 7.0 x 10^{19} cm^{-3}, and the 500Å thick n-layer phosphorus concentration was 2.0 x 10^{20} cm^{-3}, as measured by SIMS. The a-Si:H layers are formed by very high rate PECVD deposition methods (> 30 Å/s), with the resultant films having an intrinsic defect density of < 4 x 10^{15} cm^{-3} [5].

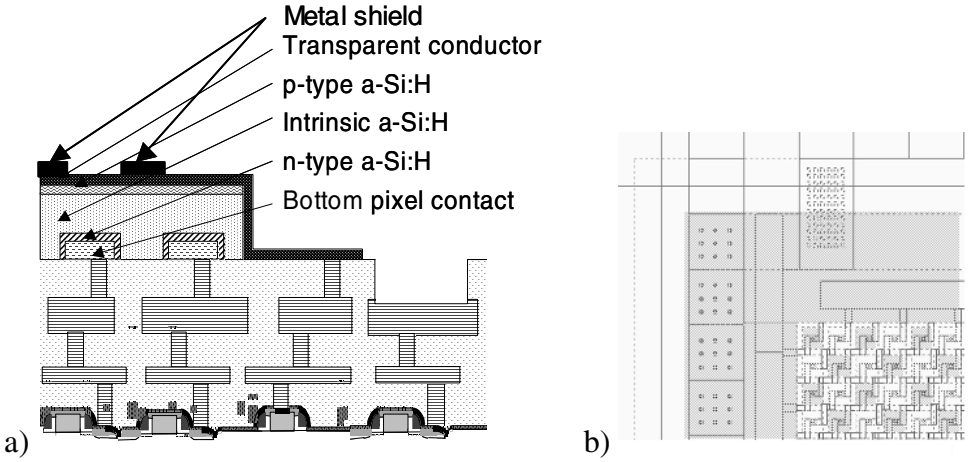


Figure 1: a) Schematic diagram of elevated a-Si:H photodiodes. The metal shield lies over the region between adjacent pixels. It is absent in the control arrays. The transparent conductor overlies the entire structure as well as the p-type contact (P). b) Layout of a corner of the pixel array. The pixels are connected into two interpenetrating checkerboard diode arrays (CTR1, and CTR2) surrounded by an independently biased guard-ring (R1).

a) b)

Figure 2: Equipment configuration for the transient photocurrent experiment, a) interpixel transient photocurrent setup, b) junction bias setup.

Measurements were made by pulsing light from a red LED onto the photodiode and monitoring the current decay as a function of time, for various bias configurations using an Agilent 4156B. In one set of experiments, referred to as junction biasing, the bias between the pixels is held to zero, while the overall bias between the common p-type junction and the pixel is varied. For the other set of experiments, referred to as interpixel biasing, the diode is held under reverse bias with respect to the common p-type junction, with various biases applied between the adjacent pixels. A light pulse is generated with a red (Agilent p/n HLMP-EP15, λ_{pk}~630nm) LED connected to an external dc power supply through HP 3488 switch. In these experiments, the Agilent 4156B was put into a sampling mode in which data was collected every 0.1s, and the current was monitored from the point at which the diode bias was switched from 0V to the set bias. All measurements were made in complete darkness and a sample temperature of 21°C.

The transient photocurrent measurements are conceptually quite simple. Once the appropriate biases are applied to the diode, data collection begins, and the light is pulsed. The fall time for the photocurrent is measured as the time from when the LED light is turned off until the value of the photocurrent drops below 1 x 10^{-11} A. Light pulses of durations from 3 seconds to 30 seconds showed a constant decay behavior, therefore light pulse of 3 seconds were used for the experiments. The LED forward drive bias was set to 2.0V.

3 RESULTS

Figure 3 shows the steady state leakage current through the junction at various electric fields. For the experiments shown here the highest reverse junction bias is 1V, for 5500Å junctions, the 17 pA/cm^2, or 150fA for a topographically planar junction. Given the field enhancement caused by topography and terminated pixels is about 20x, then the maximum injected current is ~3.0 pA [6], and the edge array injected current is ~1.5 pA, so that the current measured at ICT1R1 in the following figures is predominantly junction leakage and photocurrent.

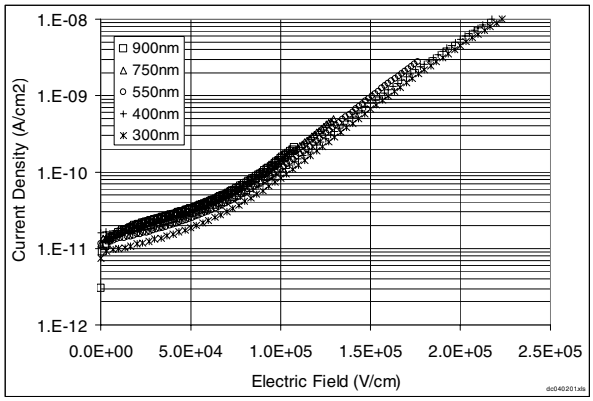


Figure 3: Current density as a function of electric field for an a-Si:H diode series with the same layout but different i-layer thickness.

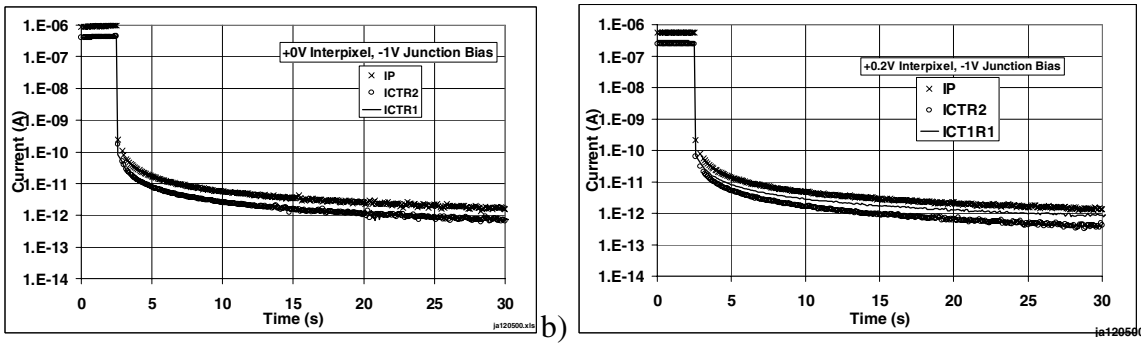


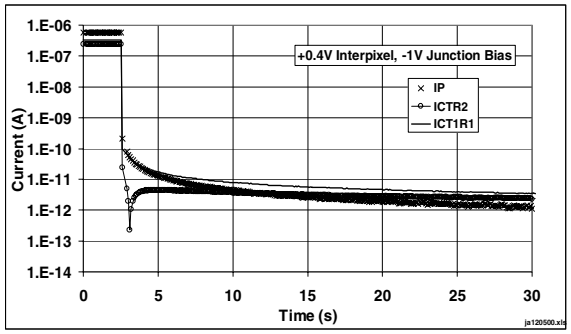
Figure 4: a) Transient photocurrents through the three terminals of the photodiode array, at –1.0V reverse bias across the junction. b) Transient photocurrents through the three terminals of the photodiode array, at –1.0V reverse bias across the junction between ICT1R1 and P, and +200mV bias of ICTR2 w.r.t. ICT1R1.

Figure 4a shows the photocurrent decay as a function of time when the diodes are held under a constant reverse bias. After an initial rapid decline one the light source is removed, the transient response shows the classical logarithmic decay indicative of deep-trap emission, as shown by Wieczorek and Fuhs [7]. In this experiment, the current is evenly balanced between the common P electrode and the two n-type junction channels ICTR2 and ICT1R1. Given that ICT1R1 is also

connected to the guard ring, which has been shown to have very high leakage currents through the array edge [1,8], it shows the transient currents are much larger than the injected currents for this timescale and thus may be neglected for the purpose of these experiments. From a practical point, Figure 4 shows the behavior a photodiode array would see under constant voltage circuit operation.

Figure 4b shows the a similar experiment in which CTR2 has a +200mV bias relative to CTR1/R1, and 800mV reverse bias relative to P. Looking very closely between Figure 4a and figure 4b, one can discern that there is a very slight decrease in the current flowing through P, a marked decrease in the current flowing through ICTR2 and an increase in ICTR1/R1.

a)



b)

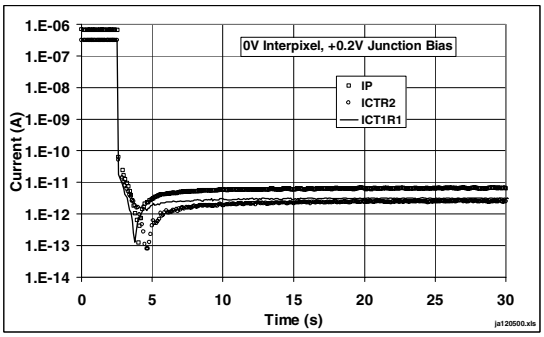
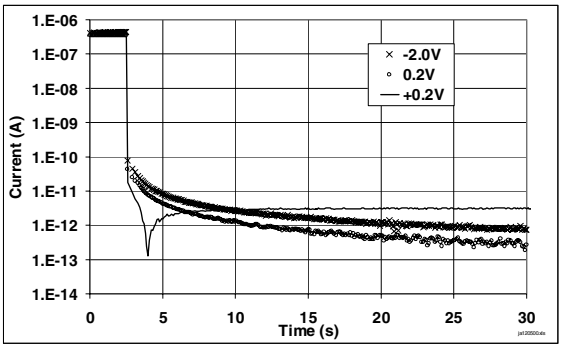


Figure 5: a)Transient photocurrents through the three terminals of the photodiode array, at -1.0V reverse bias across the junction between ICT1R1 and P, and +400mV bias of ICTR2 with respect to ICT1R1. b) Transient photocurrents through the three terminals of the photodiode array, at +0.2V reverse bias across the junction.

Figure 5a shows a more pronounced effect at CTR2 at +400mV relative to CTR1/R1, and 600mV reverse bias to P, and shows very interesting behavior at the three terminals. In this case, one sees that a large steady state current is measurable through ICTR2 after about 1200 msec. The current through CTR1/R1 is now higher than through CTR2, and both have steady state values higher than P. This is interpreted as follows. 1) The initial decline in ICTR2 current is due to a faster reduction in photocurrent, 2) whereas the steady state value for ICTR2 is dominated by and injected current *between* the pixels. This is further evidenced by the magnitude increase seen in the ICTR1R1 current, which appears to be added to the transient photocurrent for this terminal.

Figure 5b shows the effect of holding both CTR2 and CTR1R1 at 0 bias relative to one another, but at a slight forward bias relative to P. Once again in this figure, it is interpreted as an initial drop in the photocurrent, which is quickly replaced with a steady state injected current. In this experiment one sees that each of the photocurrent decay at each terminal is the same and much faster than seen in Figure 4a. In this circumstance, since there is no bias between the pixels, there is no current flow between them, but rather through the junction. As one can see the current through CTR2 and CTR1R1 are equal and both add up to equal the current through P.

Figure 6a shows photocurrent decay plots for three different junction bias conditions. Under reverse bias conditions from –2.0V down to 0V, there is a small but noticeable decrease in the characteristic time for the photocurrent transient, however a forward bias of only 200mV forward bias drastically decreases the decay time. The characteristic decay exponent (τ) of photocurrent found from the slope of a log-log plot of current versus time, for various junction biases is plotted in Figure 6b, and shows a clear transition in τ as a function of bias with the inflection point at 0.0V.

a) 

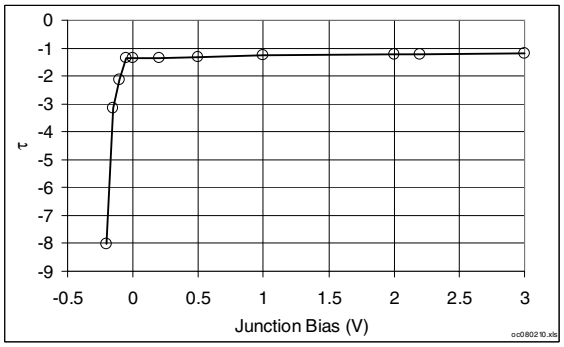
b) 

Figure 6: a) Transient photocurrent decay through the pixel as a function of junction bias. Note the large drop in decay time for a small forward bias relative to the small decrease as a function of reverse bias. b) Transient photocurrent decay exponent as a function of junction bias from 3.0 down to -0.2V.

4 DISCUSSION

It is quite likely that the residual photocurrent remaining within the i-layer consists of the trapping of carriers in deep-level states. For the minimum timescale of measurements presented here (~10^{-1}s), it can be assumed that the residual charge extracted from the i-layer has been thermalized into deep-level, localized states [9]. The low-defect density (~600Å mean defect separation) of the material implies that trapped charge is spatially isolated, since the mean trapping distance is ~10Å [10]. Additionally, since thermalization leaves trapped charge in a potential well on the order of several tenths of an eV, recombination between trapped carriers takes place at an extremely low rate [11]. Therefore it is generally believed that trapped carrier recombination occurs through free-carrier capture. Carriers injected into the i-layer initially have high enough energy that they can traverse extended states or shallow localized states attracted towards trapped charge through Coulombic forces.

What is most interesting however, is the phenomenologically different transient decay behavior of the different electrodes during interpixel biasing, which can be thought of as an n-i-n device. When the 400mV interpixel bias is applied across the 1 μm space between pixels, the generated current reduces the photocurrent for the less negative pixel, but increases the photocurrent for the more negative pixel. The interpixel bias diverts a portion of the injected current from more negative pixel, thus reducing the recombination rate. On the other hand, the additional current in the less negative pixel enhances the recombination rate. The current increase in the more negative pixel comes from attraction of a portion of the hole bias, while the decrease in the lower bias pixel current comes from electron transport across the interpixel region. The electron injection is an opportunity for hole annihilation, as there is a probability of EHP recombination.

Field effects and current injection can explain the effect of the junction bias on photocurrent decay. Under forward bias conditions, the magnitude of injected current is quite large and therefore provides a source of carriers for recombination. Counter-intuitively though, while the contribution to reverse bias currents (contact injection, thermal generation, and field–assisted tunneling), increase as a function of reverse bias, it is observed that the photocurrent decay time also increases. One explanation to this paradox is that the increasing electric field tends to decrease the recombination rate by reducing the carrier transit time across the junction. However, as seen in Figure 6b, the effect is weak.

The results of the experiments show both a practical benefit of controlling the bias between different diode array elements, as well as highlighting some interesting phenomena of a-Si:H diodes. The practical benefit is that it may be possible to decrease the characteristic decay time by at least a factor of 10, by placing a few hundred millivolts field between two pixels (interpixel bias). Additionally switching the biasing of the junction from reverse to small forward bias can produce decreases in the characteristic time by as factor of 10 as well. Such a reduction in the decay time would suppress the junction contribution to image lag below decay times of other system components, such as circuit operation issues. There are several ways in which one might imagine methods in which the photocurrent transients can be reduced in an image sensor. One method would be to pulse the interpixel bias between pixels so that holes are eliminated in one portion of the array, the switch the bias sign to eliminate holes in the other portion of the array. Another method would be to apply a brief forward bias pulse to the array to inject enough charge to annihilate the remaining holes, then switch back to reverse bias to extract the remaining electrons.

5 SUMMARY

In this work is has been shown that currents injected into or between elements of an a-Si:H photodiode array modulate photocurrent decay, either by 1) charge transfer of injected currents between pixels, or 2) massive current injection from forward biasing the diode. In both schemes, it is possible to decrease the characteristic decay time by 10x. It appears that the process by which this occurs, is by electron injection and subsequent trapped hole annihilation. The practical result is that it is possible to control the degree of lag currents contributed by the a-Si:H photodiode, so that it is not the limiting factor with respect to lag in CMOS image sensor development.

REFERENCES

[1] J. A. Theil, R. Snyder, D. Hula, K. Lindahl, H. Haddad, and J. Roland, *J. Non-Cryst. Sol.,* **299**, 1234 (2002).

[2] J. A. Theil, M. Cao, G. Kooi, G. W. Ray, W. Greene, J. Lin, A. J. Budrys, U. Yoon, S. Ma, and H. Stork, *MRS Symp. Proc.,* **609**, A14.3.1 (2000).

[3] H. Fischer, J. Schulte, P. Rieve, and M. Böhm, *Mat. Res. Soc. Symp. Proc.*, **336**, 867 (1994).

[4] J. A. Theil, H. Haddad, R. Snyder, M. Zelman, D. Hula, and K. Lindahl, *Proceedings of the SPIE*, **4435**, 206 (2001).

[5] J. Theil, D. Lefforge, G. Kooi, M. Cao, and G. Ray, *J. Non-Cryst. Sol.,* **569** 266 (2000).

[6] J. A. Theil, *Mat. Res. Soc. Symp. Proc.,* **762**, 21.4 (2003).

[7] H. Wieczorek, and W. Fuhs, *Phys. Stat. Sol. (a),* **109**, 245 (1988).

[8] J. A. Theil, *IEE Proc. Circuits, Devices, and Systems*, **150**(4), accepted for publication (2003).

[9] R. A. Street, *Hydrogenated Amorphous Silicon*, (Cambridge University Press, 1987) pp 288-292.

[10] R. A. Street, *Phys. Rev.,* **B27**, 4924 (1983).

[11] N. Schultz, B. Yan, A. Efros, and P. C. Taylor, *J. Non-Cryst. Sol.*, **266**, 372 (2000).