DEVELOPMENT OF LOW TEMPERATURE DIRECT BOND INTERCONNECT TECHNOLOGY FOR DIE-TO-WAFER AND DIE-TO-DIE APPLICATIONS—STACKING, YIELD IMPROVEMENT, RELIABILITY ASSESSMENT

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ABSTRACT
The Direct Bond Interconnect technology (DBI), commonly referred to as low temperature hybrid bonding, is an attractive bonding technology with the potential of much finer pitch and higher throughput than any solder based microbump bonding. Dielectric bonding takes place at ambient temperatures while the metal interconnection (usually Cu to Cu) forms at low annealing temperatures ranging from 150ºC to 300ºC. A 6µm pitch process is currently in high volume production for wafer-to-wafer (W2W) hybrid bonding.

Die-to-wafer (D2W) and die-to-die (D2D) assembly has been in development at Xperi. The unique challenges include producing shallow, uniform and well controlled Cu recess on Cu bond pads of 5 um or greater, which is substantially larger than what is normally used in W2W bonding and particle minimization on die surface prior to bonding. Xperi-designed daisy chain dies and wafers consist of chains ranging from 2 to 31356 interconnects. Die size is 7.96 mm by 11.96 mm, which is similar to a typical high bandwidth memory (HBM) die. The bonding studies include 10µm and 15µm diameter bond pads on 40µm pitch and 5µm diameter bond pads on 10µm pitch. The die thickness is either 50 µm or 200 µm.

In this paper, we present the latest development of our chemical mechanical polish (CMP) technology to produce uniform shallow Cu recess on 15um circular bond pads. The large pad size allows for a relaxed alignment accuracy requirement similar to manufacturing high throughput flip chip bonders available today. Additionally, high volume production ready process for bonding and D2W multi-layer stacking are explored as well as bonding yield and reliability improvement results.

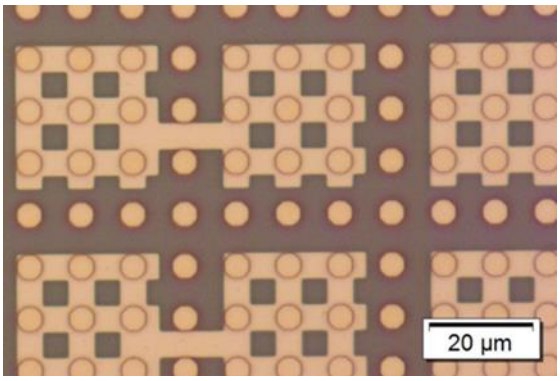
Key words: Cu-to-Cu bonding, hybrid bonding, DBI®, D2W, D2D, die stacking, 3D, 2.5D

INTRODUCTION
Requirements for higher I/O density and performance at lower cost is projected to drive the 2.5D or 3D interconnection pitch to 20µm and below in the next 5 years. Since solder interconnect technology is fundamentally challenged to deliver high volume manufacturing solutions to meet such requirements [i], [ii], the search for alternatives continue.

One promising technology is the DBI® technology, or low temperature hybrid bonding[iii, iv ,v], which forms a dielectric-to-dielectric (SiO_2-to-SiO_2 for this study) bond at room temperature and then establishes metal-to-metal connection (usually Cu-to-Cu) by a low temperature batch annealing process (150 – 300ºC). The technology has been in high volume production for wafer-to-wafer (W2W) bonding since 2015[vi]. Die-to-wafer (D2W) bonding of the same technologies has some unique challenges. In conjunction with previous publications [vii, viii, ix, x], we continue to share the development and readiness of this technology for ramp into high volume production.

TEST VEHICLE DESIGN
The objectives in the test vehicle design are to demonstrate feasibility of pitch scaling from 40um to 10 um and the compatibility of the D2W hybrid bonding technology using existing high volume flip chip assembly infrastructure with alignment accuracies of 5-10 µm. Daisy chain dice of 7.96 mm x 11.96 mm for this D2W bonding and stacking study (Figure 1) were chosen to mimic a typical HBM die. The die has Cu patterns embedded in oxide specially designed for direct bonding. Initial bonding process development used wafers with a single bonding surface. Stacking studies required die fabricated from double-sided bonding wafers. Die thickness includes both 200µm and 50µm.
Design A (Figure 1a) uses 5µm circular Cu pads for bonding. The surface is populated uniformly with such

pads in 10 µm pitch to maintain CMP uniformity. A grid structure in the underlining Cu re-distribution layer (RDL) connects nine Cu pads in the bonding layer together for each daisy chain link. The design is well suited to demonstrate bonding at 10µm pitch, however, it requires bonder alignment accuracy of +/-2.5µm. After developing advanced CMP technology to enable design of larger bonding pads with uniform recess across the wafer, we relaxed the alignment accuracy of the pick and place tool. For design B shown in Figure 1b, the bond pad size is 10µm. For design C shown in Figure 1c, the bond pads are 15µm in diameter. The three designs share the same RDL layer pattern and pitch of 40 um for comparison of results.



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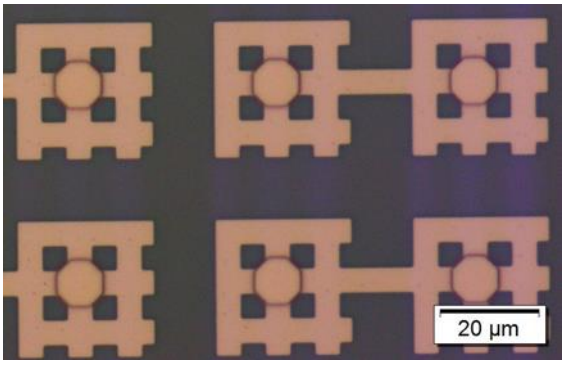

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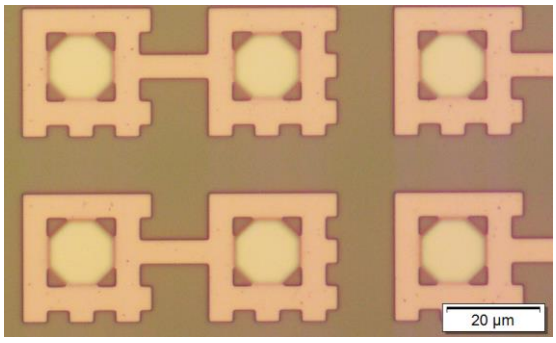

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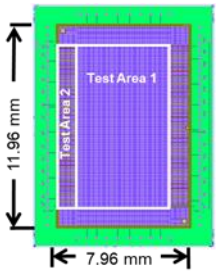
Figure 1: Optical images of circular Cu bond pads and grid RDL layers in different test vehicle designs. (a) Design A: 5µm circular bond pads on 10µm bonding pitch with 40um RDL pitch; (b) Design B: 10µm circular bond pads on 40µm bonding pitch and RDL pitch; (c) Design C:15µm circular bond pads on 40µm bonding pitch and RDL pitch.

The mating die size on the host wafer is larger in the x-axis to accommodate the probe pads for electrical testing. The wafer fabrication process described in a previous publication [vii] is scalable to 300mm. Test areas on the bonded D2W structure are shown in Figure 2. The main daisy chain in test area 1 has 31356 links and covers 50mm^2 of bonding area. Daisy chain continuity results reported in this paper are from this test area. As mentioned earlier, we keep the RDL pitch constant for all three designs. As a result, design A has 9 redundant pads for each RDL link, whereas design B and C have no redundant pads.



Design	Pad Size (um)	bond Pitch (um)	Pads/RDL Unit	RDL Pitch (um)
A	5	10	9	40
B	10	40	1	40
C	15	40	1	40

(a) **(b)**

Figure 2: (a) Illustration of the daisy chain test structures. Test area 1 covers 50mm^2 area and has 31356 links. (b) Comparison of the three designs. Design A has 9 bond pads on each RDL grid. Design B and C has only one bond pads on each RDL grid.

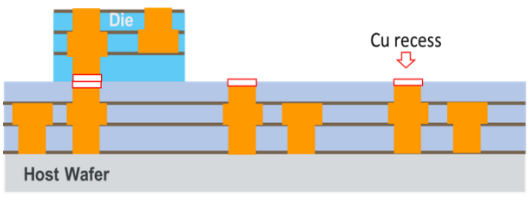
CMP PROCESS DEVELOPMENT

Controlling the bonding surface roughness and Cu recess from the oxide is critical for high assembly yield of low temperature hybrid bonding. The first stage of the bonding is the formation of oxide-to-oxide bond at ambient condition with minimal external pressure. It requires very smooth surface with a sub-nanometer roughness. The metal bond pads are recessed from the dielectric surface, as illustrated in Figure 3a. The bond strength at the ambient condition is strong and holds the

die in place for all handling until annealing is complete. During anneal, the Cu pads expand more than the surrounding oxide and bridge the gap between the two metal surfaces to form a permanent Cu- Cu bond. Since larger recess requires higher anneal temperatures to bridge the gap, controlling the depth and uniformity of the metal recess across the entire wafer is critical for achieving high assembly yield at anneal temperature below 300°C.

The CMP process for Cu damascene process commonly available in silicon foundries today can meet the oxide surface roughness for hybrid bonding. However, the strict Cu recess requirements for large circular pads can be challenging at the CMP process. One phenomena common in Cu CMP is an increase in the depth of the Cu dishing as the Cu feature size increases. Via and traces for the silicon back-end-of-line (BOEL) are mostly at submicron dimension and therefore dishing is naturally shallow. For BEOL fabrication process, large Cu features are used in test pads for electrical probing. Cu dishing in the range of hundreds of nm does not affect electrical test. Therefore, standard CMP processes are not optimized for controlling dishing on large pads for the direct bond application.

We have developed unique CMP processes that produce shallow and uniform Cu recess across 200mm wafers as part of our D2W and D2D direct bond interconnect technology development. Our CMP process yields shallow and uniform Cu recess for the following bond pad sizes up to 15 um. We have experimentally verified the following dimensions: 1 µm line width in a 20µm grid pattern, and circular pads with diameters of 2µm, 3µm, 5µm, 10µm and 15µm. As shown in Figure 3b, we can control the variation of Cu recess of 15 µm diameter circular bond pads to less than 2.5nm across a 200um wafer. We have also demonstrated good bonding yield with such Cu recess. The process was transferred to high volume CMP equipment for 300mm wafers with equivalent Cu recess after CMP.



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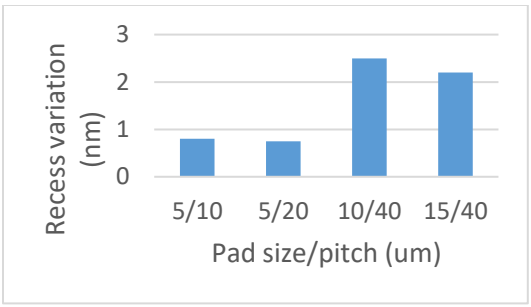


(b)

Figure 3: (a) Illustration of Cu recess after D2W bonding interface before anneal. (b) Standard deviation of Cu recess on the DBI bonding surface from the mean value of the same wafers. AFM measurements were taken from 9 points on the wafer, two measurements at each point (forward and backward scans)

WAFER AND DIE PREPARATION AND BONDING

Preparation of the host wafer for the first layer bonding is the same as for W2W bonding. The wafer surface is very clean after the final CMP press used to produce smooth oxide surface and specific Cu recess. A rinse in deionized (DI) water and a plasma activation process complete the wafer preparation process.

The die singulation process generate particles, contaminants, and edge defects. Consequently, the die preparation process requires more cleaning effort than in a wafer format. Die handling steps also add contamination if the process is not well designed and controlled.

Figure 4 shows the two process flows used in our development: the prototype process flow and the production ready process flow. We used the prototype process flow to understand the fundamentals of D2W bonding. In this process flow, we place die with protective coating into a custom designed tray. A wet clean process removes the coating on the die surface. After the coating removal, die surface activation completes in a plasma process. Activated die are bonded to the host wafer with a Toray flip chip bonder with an alignment accuracy of +/-2µm.

After bonding the first layer of die, additional die stacking or final anneal may commence. For stacking, the backside of the bonded die are cleaned and activated, and the steps for die picking, cleaning, activation and bonding are repeated for the additional bonding

sequence. Once the desired number of die stacks are achieved, the host wafer receives a final anneal process. The Cu-to-Cu interconnect across the entire stack is formed during the final anneal process. Since the Cu bond pads are completely surrounded by bonded oxide surface and there is no exposure to the environment in the oven, Cu oxidation in the bonded area is not a concern. Therefore, anneal may be carried out in air unless there are exposed Cu pads outside of the bonded area on the host wafer.

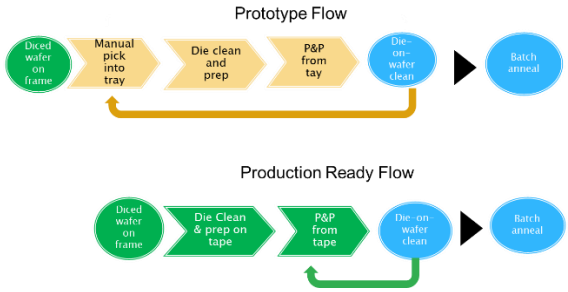


Figure 4: Illustration of the prototype D2W bonding process flow and the production ready process flow

The prototype flow provides a platform to gain understanding of the die cleaning and bonding requirements. The production ready flow development addresses the engineering requirements for high throughput assembly. In the production ready flow, we eliminate manual picking of the die and custom trays for die preparation. Instead, the dicing tape on frame serves as the carrier for all die preparation prior to entering the pick and place tool. Figure 5 shows a diced 200mm wafer on frame that is cleaned and ready for bonding.

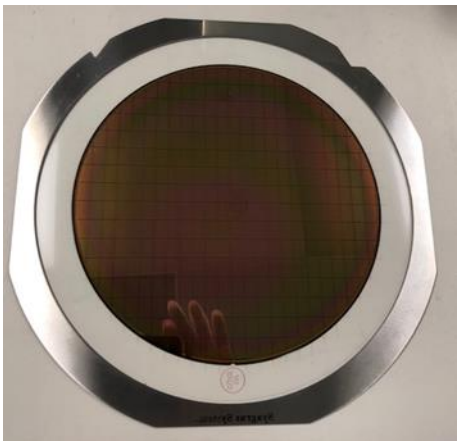
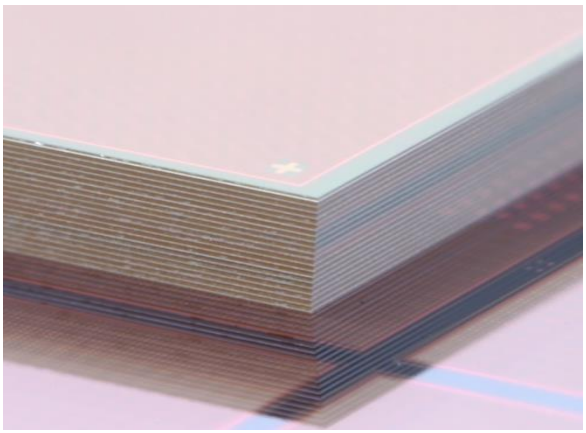


Figure 5: Picture of a diced 200mm wafer cleaned and activated on dicing frame and ready for bonding.

In our study, we used a Datacon Evo 2200 to pick the die directly from the frame and flip it for bonding. We have reported that the bonder can run at full speed specified by the equipment manufacturer since the bonding process is spontaneous [ix].

We have shown images and cross sections of D2W bonded parts for single layer and 4-high die stacks previously. Figure 6 shows a picture and cross-section of a 20-die stack on a host wafer. The stack height is the sum of total die thickness only. In this case, the die are 50um thick and the stack height is 1mm. In addition to minimizing stack height, the removal or organic material between die enhances heat transfer through the stack and thermal and electrical specifications [viii]. By eliminating the solder and under-fill between layers, the assembly process streamlines, the stack height reduces and the overall performance improves.



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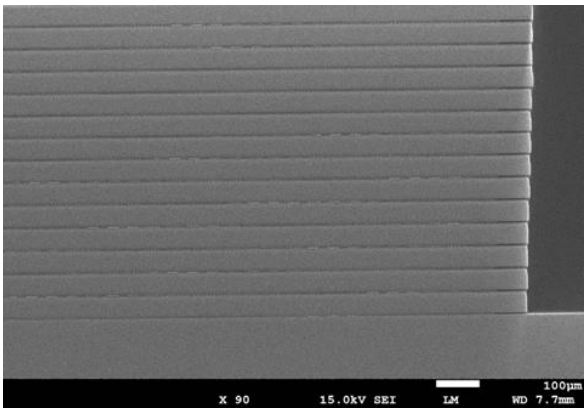

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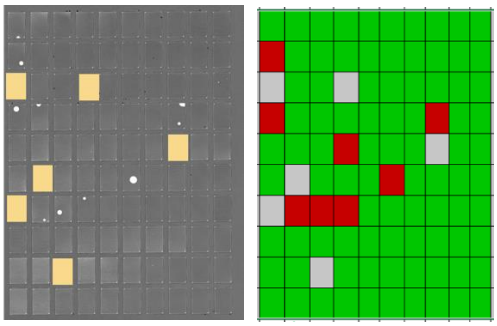
Figure 6: (a) Picture of a 20-die stack on a host wafer. Die thickness is 50um, stack height is 1mm; **(b)** Cross-section of the 20-die showing oxide and Cu hybrid bonding structure.

D2W BONDING YIELD IMPROVEMENT

Figure 7 shows an image from confocal scanning acoustic microscopy (CSAM) and electrical continuity test results from an experimental lot. A 10x10 bonding array is designated on the host wafer using the die and wafer from design B with a single bond pad for each link. Six defective sites in the host wafer array skipped during bond are colored in light yellow (Figure 7). The CSAM image showed 8 dies with bonding voids in the large test area 1 shown in Figure 2a. Electrical continuity tests show open circuit for the same 8 die with voids. The correlation between interface void and electrical open is 100%. The Cu recess variation across the wafer does not impact assembly yield, which is important for high volume assembly.



(a) (b)

Figure 7: (a) CSAM image of Design B dies bonded to a host wafer in a 10x10 array. The defective sites skipped during bond are colored in yellow; (b) Corresponding electrical continuity results for the daisy chain test area 1 with 31356 links. Green indicates electrical continuity and red indicates electrical open.

The likely cause of bonding voids in Figure 7 is contamination on the host wafer or die bonding surface. We developed cleaning processes and die handling protocols to minimize particle contamination. These improved measures increase the bonding yield over time as shown in Figure 8.We have achieved greater than 90% yield in a 1K clean room prototype laboratory with manual operation of most equipment. Therefore, we expect that a production environment with automated wafer and die handling will enable higher yields required by the industry standards for volume manufacturing.

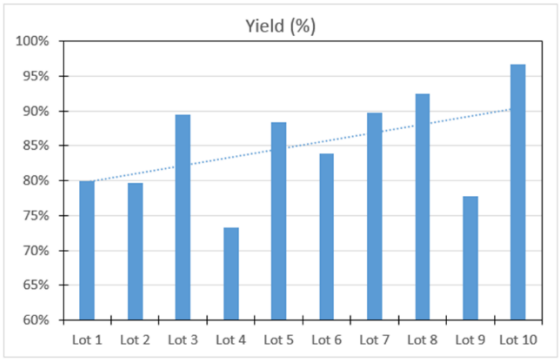


Figure 8: Time-sequenced bonding yields of 10 experimental lots measured by electrical continuity of the daisy chain in test area 1 with 31356 links.

RELIABILITY TEST RESULTS

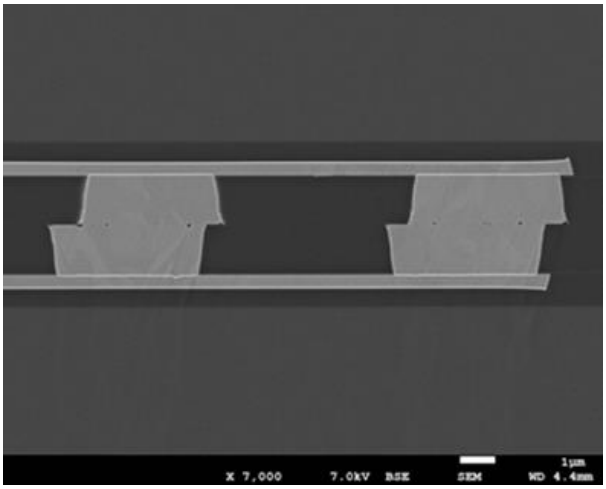
After resistance measurements at the water level, we dice the wafer and put the diced parts through the following reliability tests: temperature cycling, high temperature storage at two different conditions (225ºC and 275ºC) and autoclave test. Table 1 gives a summary of the results from 4 different lots.

The temperature cycling test specification used was JESD22-A104D Condition M (from -40ºC to 150ºC). The JEDEC requirement is 1000 cycles with a resistance increase less than 10%. At 1000 cycles, the resistance dropped slightly as expected with a single component interconnect. There is no driving force for intermetallic formation. We extended the test to 2000 cycles, and the resistance dropped further. The decrease in most dies is 1.5–1.7%, with one exception of 3.4% drop on one die. In Figure 9, the cross section of one die post temperature cycling test is compared with a cross sectioned die without any temperature cycling exposure. The quality of bonding interface for the two dies look very similar. The die interconnects after 2000 cycles of testing show no indications of thermal fatigue. With no CTE mismatch between the top and bottom die of the bonded joints, there is no driving force for crack initiation. The hermetic bonded oxide areas keep the Cu joints free from any oxygen in the environment resulting in no Cu oxidation. In fact, the extended exposure to higher temperature serves as additional annealing for the Cu joints, potentially reduces micro voiding at the bonding interface and causes the small decrease in the daisy chain resistance. The quality of the single component Cu interconnects promises to delivery more reliable improved thermal performance in stacked die packages like memory and system on chip (SoC) in the electronics.

Two sample sets with 22 units each were tested to the JEDEC requirements (< 10% resistance increase for up to 1000 hours) for high temperature storage test at 225ºC and 275ºC, respectively. Both lots were tested for 1000 and 2000 hours to examine any trends. All 44 parts showed a slight resistance drop of at least 1.2-1.4% after 2000 hours of test (twice the required duration). Across section of a part from each group showed a pristine Cu interconnect.

Table 1: Reliability test results for Design A of D2W assembly

Test	Standard	Test Condition	Sample size	Result
Temperature Cycling (Board Level)	JESD22-A104D Condition G	-40°C to 150°C, 2000 cycles	45	Pass
High Temperature Storage	JESD22-A103	225°C, 2000 hours	22	Pass
High Temperature Storage	JESD22-A103	275°C, 2000 hours	22	Pass
Autoclave	JESD22-A102D	121°C/100%RH, 15psi, 168hrs	22	Pass



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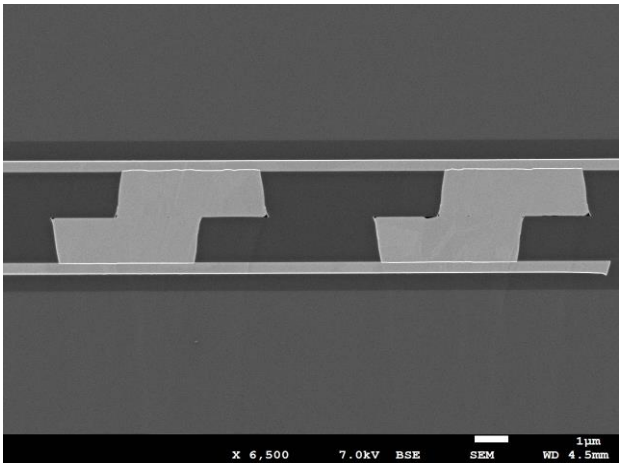

(b)

Figure 9: Cross-section image of Cu-to-Cu joints. (a) Part with no exposure to reliability testing; (b) After 2000 cycles of temperature cycling test.

Another set of 22 die went through 168 hours of autoclave test at 121ºC and 15 psi vapor pressure. All parts showed no resistance increase and no sign of Cu corrosion. A second benefit of the direct bond interconnect technology in reliability performance is the hermetic seal provided at the dielectric-dielectric and the Cu-Cu bonded interfaces. The interconnect performance in environmental stress testing such as temperature cycling, high temperature storage and autoclave exposure makes hybrid bonding the ideal choice for high performance applications in harsh environments such as high power high performance computing or under-hood environment for automotive electronics.

SUMMARY

Low temperature direct bond interconnect technology enables interconnect pitch scaling to a submicron level. Two critical challenges for direct bond in D2W applications are managing Cu dishing on large bond pads and minimizing surface contamination during the assembly process. We demonstrated that both engineering challenges have been addressed successfully. An HVM CMP process is demonstrated at both 200mm and 300mm to achieve shallow and uniform Cu recess in bond pads as large as 15µm diameter. Thin die handling and bonding processes were developed on HVM compatible equipment demonstrating contamination control.

The flexibility of this technology is apparent with the demonstration of a 20-die stack with hybrid bonding. The single daisy chain die all passed the environmental

stress tests including temperature cycling, high temperature storage and autoclave testing. All parts showed superior performance with no increase in resistivity, no crack initiation or defect growth. Finally, the superior reliability performance of the Cu direct bond interconnect illustrates the promise of this next generation interconnect.

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