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Hydrogenated Amorphous Silicon Photodiode Technology for Advanced CMOS Active Pixel Sensor Imagers

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ABSTRACT

Amorphous silicon photodiode technology is a very attractive option for image array integrated circuits because it enables large die-size reduction and higher light collection efficiency than c-Si arrays. We have developed a photodiode array technology that is fully compatible with a 0.35µm CMOS process to produce image sensors arrays with 10-bit dynamic range that are 30% smaller than comparable c-Si photodiode arrays. The VGA (640x480), array demonstrated here uses common intrinsic and p-type contact layers, and makes reliable contact to those layers by use of a monolithic transparent conductor strap tied to vias in the interconnect. The work presented here will discuss performance issues and solutions that lend themselves to cost-effective high-volume manufacturing. The various methods of interconnection of the diode to the array and their advantages will be presented. The photodiode dark leakage current density is about 80 pA/cm^2, and its absolute quantum efficiency peaks about 85% at 550 nm. The effect of doped layer thickness and concentration on quantum efficiency, and the effect of a-Si:H defect concentration on diode performance will be discussed.

INTRODUCTION

Active pixel sensors are an attractive alternative to CCD image sensor because of lower power consumption, random pixel access, and a higher degree of system integration which often lead to reduced overall system costs [1]. Several advantages could be realized by elevating the photodiode above the substrate such as, resolution improvements, maximizing the light collection area, introduction of more efficient semiconducting layers, and minimizing absorption of light from intervening layers. While elevated photodiode arrays on CMOS and CCD technologies have been demonstrated, acceptance has been slow due to potentially expensive manufacturing techniques such as low a-Si:H deposition rates, and complex

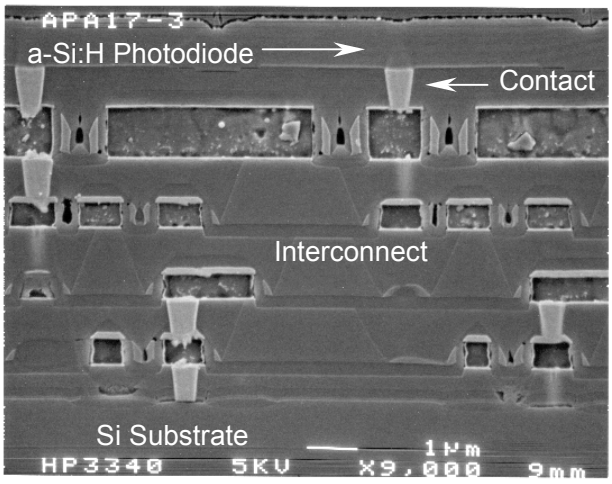

Figure 1: SEM cross section of elevated photodiode.

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upper contact schemes; and process control-limited designs such as step coverage pixel isolation [2-7].

An elevated sensor technology utilizing hydrogenated amorphous silicon photodiodes has been developed that overcomes all of these concerns. The features of this technology allow for deposition rates of a-Si:H that are high enough to permit cost-effective manufacturing, contact with the top side of the diode is monolithic, and a process flow that allows for well controlled isolation of the pixel contact layer. In addition, the performance of the diode exceeds that of a c-Si diode in some ways. For example, the absolute quantum efficiency of the photodiodes is about 85% in portions of the visible wavelength regime, and the leakage current from the diode can achieve 80 pA/cm^2.

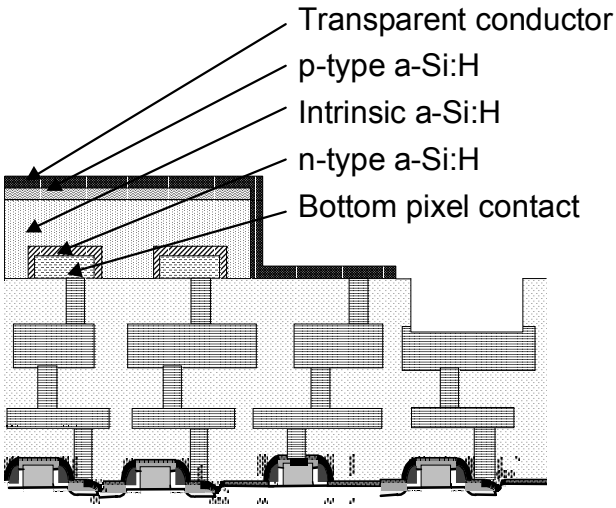

Figure 2: Drawing of elevated photodiode array cross-section.

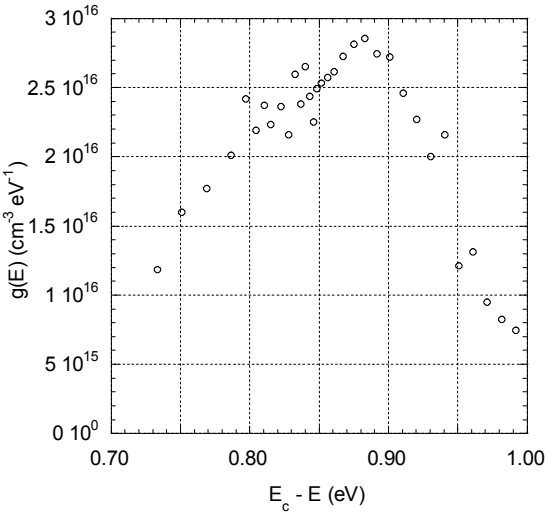

Figure 3: Deep-level density of states plot of a-Si:H used for these experiments.

ARRAY DESCRIPTION

The photodiode array is formed after standard processing, and consists of an array of n-type a-Si:H pixels with a common intrinsic and p-type a-Si:H layers that form an array of p-i-n photodiodes, (see Figure 1, and the drawing in Figure 2). Top contact to the array is made by using a transparent conductor layer that connects the top surface of the p-type a-Si:H layer to vias adjacent to the array and is referred to as the local-via monolithic interconnect (LVMI) structure [8]. The n-type a-Si:H which defines the pixel is patterned by a photolithographic and etch process sequence to ensure adequate pixel isolation. The n-type a-Si:H overlaps the bottom contact pixel metal on all sides to minimize current injection from the pixel metal. The pixel metal makes contact to standard via plugs that go through the upper isolation layer.

By allowing the transparent conductor to be in contact with the edge of the intrinsic layer for the array reduces by two the mask count for the process. This is a key point as it permits a significant simplification of the process, and associated cost reduction. This arrangement does

not degrade the imager, since a high resistance between the interface and the array can be inserted, and any excess current can be sunk by the peripheral diodes in the array.

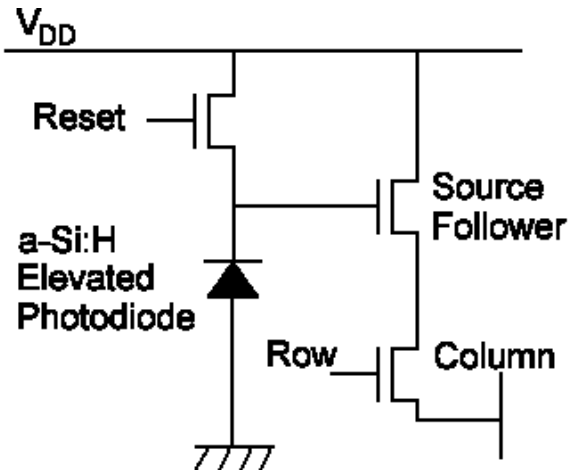

Figure 4: Source follower pixel circuit schematic .

The a-Si:H layers are formed by very high rate film deposition methods (> 30 Å/s), and the intrinsic layer is about 9000Å thick. The a-Si:H used for this sensor has an intrinsic defect density of $< 6 \times 10^{15}$ cm^{-3} [9]. Figure 3 shows the density of deep-level defects within the intrinsic layer. These measurements were carried out by the depletion transient current measurements as described in [9].

The contacting method employed utilizes standard metal vias. The via technology has advanced along with CMOS process development, so it is possible to create satisfactory vias with 0.5μm diameter. It is important that the via take up a small area relative to the pixel size to ensure minimal spacing of circuit elements below. Direct contact require tapered vias, (to alleviate step coverage concerns) through the interconnect dielectric and could easily take up 20% of a 6 x 6 μm pixel [3,7]. A standard CMOS via is made using an essentially vertical-walled cavity filled with W or Cu with a diameter of 0.5 μm. Such vias would take up less than 0.7% of the same pixel area, thus leaving the rest of the pixel area for circuit layout.

The pixel circuitry for the array is a source follower circuit as shown in Figure 4. It utilizes three NMOS FETs in a 5.9 μm square pixel, one as a reset, one as a row readout, and one as the source follower. Reference [10] provides more details of a similar circuit. The interpixel spacing is 1 μm. The photosensor is compatible a mixed signal CMOS technology and has been implemented with a 0.35 μm process subtractive aluminum process.

There are several methods by which contact can be made to the transparent conductor on top of the diode stack, both monolithic and external contact. The LVMI structure, described previously, was selected because of its low-cost and inherent high reliability. Other monolithic approaches include isolated strapping, which requires two additional masking steps and a highly selective contact etch. Another technique involves make direct contact to bonding pads. This would require wirebonding onto the transparent conductor, about which little is known for high volume integrated circuit packaging. External contact approaches include mechanical contact and direct wirebonding. However, these were rejected due to packaging and mechanical integrity of the contacts.

PHOTODIODE PERFORMANCE

The quantum efficiency for an a-Si:H photodiode across the visible spectrum is shown in Figure 5. The efficiency ranges from 40% in the blue (400nm) to almost 85% at 550nm, and

down to 15% at 700 nm. By comparison, bulk c-Si diodes have an efficiency across this range around 10-25%. Factors that lead to higher efficiency include 100% light collecting area across the pixel, and a bandgap of 1.85 eV for a-Si:H, which is more suited for collecting visible light than that of 1.1 eV c-Si.

The construction of the top diode layer is critical for optimizing the amount of shorter wavelength light that is collected. Since the upper contact layer is a non-depleted region of the diode that absorbs light and the absorption coefficient increases with shorter wavelengths it is necessary to minimize the thickness of the contact layer. On the other hand, it is necessary to maintain the depletion layer thickness to minimize charge injection from the transparent conductor layer to minimize dark current. There are two ways to minimize the depletion layer thickness, by controlling the contact layer dopant concentration, and by minimizing the doped layer thickness. Figure 5 shows that both thinning the doped layer thickness and the lowering doping level improve quantum efficiency at short wavelengths, but has little effect at longer wavelengths.

The forward bias of the current voltage characteristic (IV) curve shows an ideality of 94 mV/decade, and in reverse bias at the operating voltage of 2.5 V, the leakage current density is 80 pA/cm^2. The source of the current is attributed to trap emission, contact, and array edge leakage. Array edge leakage does not affect imager performance because it is minimized in two ways. One is to maximize the resistance between the array edge and the outermost pixel, and by collecting the leakage current using the outer row of pixels. This leakage current is comparable to that seen for advanced bulk photodiode pixels, (on the order of 10^{-10} A/cm^2.) Under 2 mW/cm^2 illumination, the photo-current density is 2.2 x 10^{-4} A/cm^2. The photo-current response is linear across this entire regime. The activation energy for thermal carrier generation is measured to be about 0.92 eV, about twice that of crystalline Si. One secondary benefit of this, is that the a-Si:H photodiode will be immune to temperature fluctuations compared with bulk diodes.

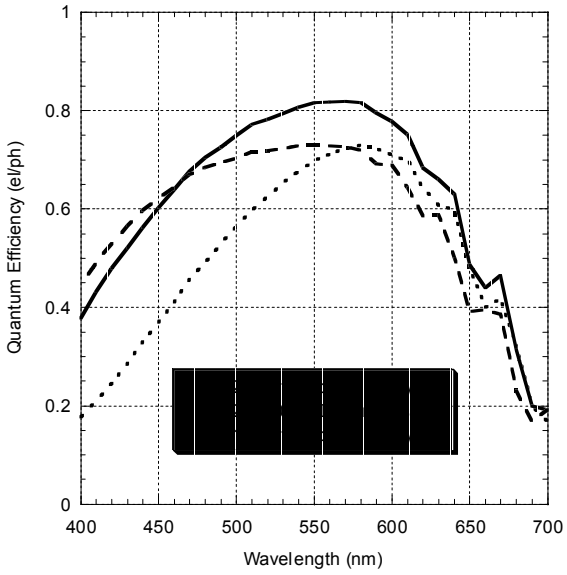

Figure 5: a-Si:H photodiode quantum efficiency as a function of p-layer a-Si:H thickness and B doping collected under -2.5V bias.

Figure 6 shows a test pattern image taken by a 10-bit VGA (640x480) elevated photodiode imager. As the image shows, all pixels are fully functional, and there is no evidence of fixed pattern noise. In addition, no blurring of edges could be found, demonstrating the photodiodes do not measurably degrade the overall circuit performance.

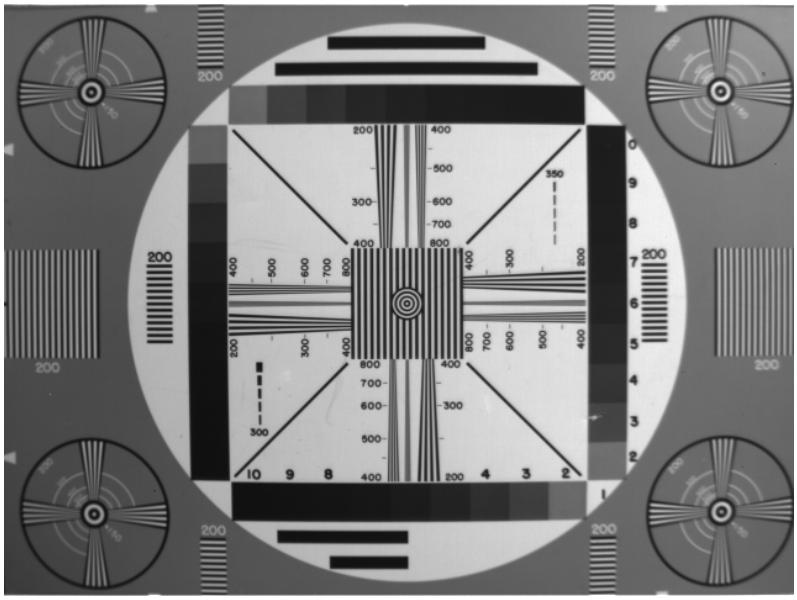

Figure 6: Test pattern image taken by a 10-bit VGA (640x480) a-Si:H photodiode array, with 5.9 μm by 5.9 μm pixels and 0.35μm CMOS process.

SUMMARY

An elevated a-Si:H photodiode array with a reliable upper electrode contact integrated with 0.35μm CMOS technology has been realized in the form of a VGA imager. The CMOS-compatible sensor technology utilizes three key features, a transparent conductor strapping design that connects the common array electrode and vias with a minimum number of masks, an etched n-type a-Si:H pixel layer, and high quality a-Si:H deposited with a very high deposition rate. Quantum efficiencies of up to 85%, and leakage current densities of 80 pA/cm^2, are obtained with diodes of this design. While a working device has been demonstrated to perform in 0.35 μm CMOS, the technology is readily extendable down to the most aggressive dimensions available. The process also is compatible with color filter processing to allow creation of color sensor arrays. In summary, it has been shown that it is possible to couple elevated semiconductor devices with standard CMOS processes to produce sensors that have at least equivalent performance to bulk silicon sensors.

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