

Performance of a-Si:H Photodiode Technology-Based Advanced CMOS Active Pixel Sensor Imagers

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ABSTRACT

Amorphous silicon photodiode technology is a very attractive option for image array integrated circuits because it enables large die-size reduction and higher light collection efficiency than c-Si arrays. The concept behind the technology is to place the photosensing element directly *above* the rest of the circuit, thus eliminating the need to make areal tradeoffs between photodiode and pixel circuit. We have developed an photodiode array technology that is fully compatible with a 0.35 μ m CMOS process to produce image sensors arrays with 10-bit dynamic range that are 30% smaller than comparable c-Si photodiode arrays. The work presented here will discuss performance issues and solutions to lend itself to cost-effective high-volume manufacturing. The various methods of interconnection of the diode to the array and their advantages will be presented. The effect of doped layer thickness and concentration on quantum efficiency, and the effect of a-Si:H defect concentration on diode performance will be discussed. The photodiode dark leakage current density is about 80 pA/cm², and its absolute quantum efficiency peaks about 85% at 550 nm. These sensors have 50% higher sensitivity, and 2x lower dark current when compared to bulk silicon sensors of the same design. The cell utilizes a 3 FET design, but allows for 100% photodiode area due to the elevated nature of the design. The VGA (640x480), array demonstrated here uses common intrinsic and p-type contact layers, and makes reliable contact to those layers by use of a monolithic transparent conductor strap tied to vias in the interconnect.

Keywords: active pixel sensors, hydrogenated amorphous silicon, elevated photodiode array, CMOS image sensors

INTRODUCTION

Active pixel sensors are an attractive alternative to CCD image sensor because of lower power consumption, random pixel access, and a higher degree of system integration, which often leads to reduced overall system costs [1]. Several advantages could be realized by elevating the photodiode above the substrate such as, resolution improvements, maximizing the light collection area, introduction of more efficient semiconductor layers, and minimizing absorption of light from intervening layers. Several attempts to create elevated photodiode arrays on CMOS and CCD technologies have been demonstrated based on hydrogenated amorphous silicon (a-Si:H) as the semiconductor [2-7]. However, acceptance has been slow due to potentially expensive manufacturing techniques such as low a-Si:H deposition rates, difficulty in maintaining clean junction interfaces, and complex upper contact schemes; and difficult to control pixel isolation integration schemes.

This article discusses the design and performance of an elevated sensor technology utilizing hydrogenated a-Si:H photodiodes which overcomes all of these concerns. The features of this technology include high a-Si:H deposition rates to permit cost-effective high volume manufacturing, contact with the top side of the diode is monolithic which is mechanically robust and minimizes fabrication complexity, and a process flow that allows for well controlled isolation of the pixel contact layer. In addition, the performance of the diode exceeds the optical performance of c-Si reverse bias photodiodes. For example, the absolute quantum efficiency of the photodiodes about 85% in portions of the visible wavelength regime, and the leakage current from the diode can achieve 80 pA/cm².

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ELEVATED DIODE ARRAY AND FABRICATION

Fabrication of the sensor starts with standard integrated circuits. At the pointing the process when the circuit undergoes passivation dielectric deposition, the dielectric is planarized to provide a flat surface on which to construct the photodiodes. The array consists of n-type a-Si:H pixels overlapping a thin metallic pixel contacts with a common intrinsic and p-type a-Si:H layers that form an array of p-i-n photodiodes, (see Figure 1 and the drawing in Figure 2). However, if desired, the process allows for the manufacture of an array with p-type pixel junctions, and a n-type common junction. Top contact to the array is made by using a transparent conductor layer that connects the top surface of the p-type a-Si:H layer to vias adjacent to the array, (monolithic top contact structure) [8]. The a-Si:H pixel is patterned by photolithographic and etch steps to ensure adequate pixel isolation. The n-type a-Si:H overlaps the bottom contact pixel metal on all sides to minimize current injection. The pixel metal makes contact to standard via plugs that go through the upper isolation layer. It should be noted that while the transparent conductor is in direct contact with the intrinsic layer, current injection has not affected imager performance. The a-Si:H layers are formed by very high rate film deposition methods ($> 30 \text{ \AA/s}$), and the intrinsic layer is about 9000\AA thick. The a-Si:H used for this sensor has an intrinsic defect density of $< 6 \times 10^{15} \text{ cm}^{-3}$ [9].

There are several methods by which contact can be made to the transparent conductor on top of the diode stack, both monolithic and external contact. The monolithic top contact structure was selected because of its low-cost and inherent high reliability, (see Figures 1 and 2). Other monolithic approaches include isolated strapping, which requires two additional masking steps and a highly selective contact etch. Alternative connection techniques involve using non-monolithic interconnections, such as wirebonding the transparent conductor to die-based or package-based bond pads. This would require wirebonding onto the transparent conductor, about which little is known for high volume integrated circuit packaging, and may impose unreasonable stresses on the a-Si:H layers. Use of mechanical clips to the transparent conductor was also considered. However, this approach suffers from deficiencies in mechanical reliability with respect to packaging and electrical integrity of the contacts.

Allowing the transparent conductor to be in contact with the edge of the intrinsic layer for the array reduces the mask count by two with respect to the isolated strapping approach. This is a key point as the two mask reduction can reduce the cost of the array fabrication by 33%. The only concern is that the contact produces a forward biased junction that injects a dark current into the array. However, this arrangement does not degrade imager, since a high resistance can be inserted between the interface and the array, and any excess current can be drawn off by peripheral diodes in the array.

The contacting method to both the pixels and the common electrode utilizes standard metal vias. Via technology has advanced along with CMOS process development, so it is possible to create satisfactory vias with $0.5\mu\text{m}$ diameter. It is important that the via take up a small area relative to the pixel size to ensure minimal spacing of circuit elements below. Direct contact require tapered vias, (to alleviate step coverage concerns) through the interconnect dielectric and could easily take up 20% of a $6 \times 6 \mu\text{m}$ pixel [6,7]. A standard CMOS via is made using an essentially vertical-walled cavity filled with W or Cu with a diameter of $0.5 \mu\text{m}$. Such vias would take up less than 0.7% of the same pixel area, thus leaving the rest of the pixel area for circuit layout.

The a-Si:H layers are formed by very high rate film deposition methods ($> 30 \text{ \AA/s}$), and the intrinsic layer is about 9000\AA thick. The a-Si:H used for this sensor has an intrinsic defect density of $< 6 \times 10^{15} \text{ cm}^{-3}$ [9]. Figure 3 shows the density of deep-level defects within the intrinsic layer. These measurements were carried out by the depletion transient current measurements as described in [9]. Electron-spin resonance of the films show that the dangling bond defect density is between 2.5 and $4 \times 10^{15} \text{ cm}^{-3}$ which is considered state of the art. The hydrogen content of the films is about 14%.

DIODE PERFORMANCE

The quantum efficiency for an a-Si:H photodiode across the visible spectrum is shown in Figure 5. The efficiency ranges from 40% in the blue (400nm) to almost 85% at 550nm, and down to 15% at 700 nm. By comparison, bulk c-Si diodes have an efficiency across this range around 10-25%. Factors that lead to higher efficiency include 100% light collecting area across the pixel, and a bandgap of 1.85 eV for a-Si:H, which is more suited for collecting visible light than for c-Si.

Figure 5 also shows that control of the upper doped contact layer controls the light collection efficiency of the shorter wavelengths. Minimizing the thickness of the p-layer and the dopant concentration of the p-layer maximizes the short wavelength efficiency as shown in Figure 5, as it allows the minimization of the depletion layer to the top surface of the diode. It is possible to increase the blue response at 400 nm from 20% to 40% across this range. Higher efficiencies could be achieved by thinning the i-layer, but this would be at the expense of red efficiency, which is limited by the absorption coefficient.

The electrical behavior of the diode is described by the IV curve shown in Figure 6. The forward bias shows an ideality of 94 mV/decade, and in reverse bias at the operating voltage of 2.5 V, the leakage current density is 80 pA/cm². The sources of the current are attributed to trap emission, contact, and array edge leakage. The array edge leakage does not affect array performance because it is minimized in two ways, one is to maximize the resistance between the array edge and the outermost pixel, and by collecting the leakage current using the outer row of pixels. This leakage current is comparable to that seen for advanced bulk photodiode pixels, (on the order of 10⁻¹⁰ A/cm².) Under 2 mW/cm² illumination, the photo-current density is 2.2 x 10⁻⁴ A/cm². The photo-current response is linear across this entire regime. The activation energy for thermal carrier generation is measured to be about 0.92 eV, about twice that of crystalline Si. One secondary benefit of this, is that the a-Si:H photodiode will be more immune to temperature fluctuations compared with bulk diodes.

SENSOR PERFORMANCE

The pixel circuitry for the array is a source follower circuit as shown in Figure 4. It utilizes three NMOS FETs in a 5.9 μ m square pixel, one as a reset, one as a row readout, and one as the source follower. The interpixel spacing is 1 μ m. The source follower circuit is the smallest circuit that provides good signal isolation. Reference provides more details of a similar source follower pixel circuit and its operation for c-Si sensor arrays [10]. The photosensor is compatible a mixed signal CMOS technology and has been implemented with a 0.35 μ m process subtractive aluminum process. Devices using 4.9 μ m square pixels have also been fabricated and provide similar performance.

Figure 7 shows a test pattern image taken by a 10-bit VGA elevated photodiode imager. No evidence of fixed pattern noise, or point defects can be seen. Also, no inter-pixel leakage as manifested by blurred edges has been detected.

SUMMARY

An elevated a-Si:H photodiode array with a reliable upper electrode contact has been realized in the form of a VGA imager. The CMOS-compatible sensor technology utilizes three key features, a transparent conductor strapping design that connects the common array electrode and vias with a number of minimum of masks, an etched n-type a-Si:H pixel layer, and high quality a-Si:H deposited with a high deposition rate. Quantum efficiencies of up to 85%, and leakage current densities of 80 pA/cm², are obtained with diodes of this design. While a working device has been demonstrated to perform in 0.35 μ m CMOS, the technology is readily extendable down to the most aggressive dimensions available. The process also is compatible with color filter processing to allow creation of color sensor arrays. In summary, it has been shown that it is possible to couple elevated a-Si:H sensor arrays to standard CMOS processes and produce sensors that are at least equivalent to bulk silicon sensors.

REFERENCES

1. E.R. Fossum, *IEDM Tech. Digest*, pp. 17, 1995.
2. B. Schneider, P. Rieve, M. Böhm, *Handbook of Computer Vision and Applications*, Vol. 1, New York: Academic Press, 1999, pp. 237-270.
3. H. Fischer, J. Schulte, P. Rieve, M. Böhm, "Technology and performance of TFA (Thin-Film on ASIC)-sensors". *Mat. Res. Soc. Symp. Proc.*, vol. **336**, pp. 867-872, 1994.
4. N. Harada, "A CCD Imager Overlaid with an a-Si:H Layer", *Amorphous Semiconductor Technologies and Devices*, pp. 283-289, 1984.
5. M. Sasaki, R. Miyagawa, and S. Manabe, *Extd. Abs. of 22nd Conf. on Sol. Stat. Dev. and Mat.*, p 705 (1990).

6. K. Tanaka, E. Maruyama, T. Shimada, and H. Okamoto, *Amorphous Silicon*, John Wiley and Sons: New York, pp. 233-235, (1999).
7. R. A. Street ed., *Technology and Applications of Amorphous Silicon*, Springer: New York, pp 161-175 (2000).
8. US Patent 6018187: Jeremy A. Theil, Min Cao, Dietrich Vook, Frederick A. Perner, Xin Sun, Shawming Ma, Gary W. Ray, *An elevated pin diode active pixel sensor including a unique interconnection*.
9. J. Theil, D. Lefforge, G. Kooi, M. Cao, G. Ray, "Mid-gap states measurements of low-level boron-doped a-Si:H films", *18th ICAMS Proc., J. Non-crystalline Solids*, **266-269**, pp. 569-573, 2000.
10. K. Singh, M. Borg, and R. Mentzer, "A High Image Quality Fully Integrated CMOS Image Sensor", *PICS 1999: Image Processing, Image Quality, Image Capture, Systems Conference*, pp. 61-65, 1999.

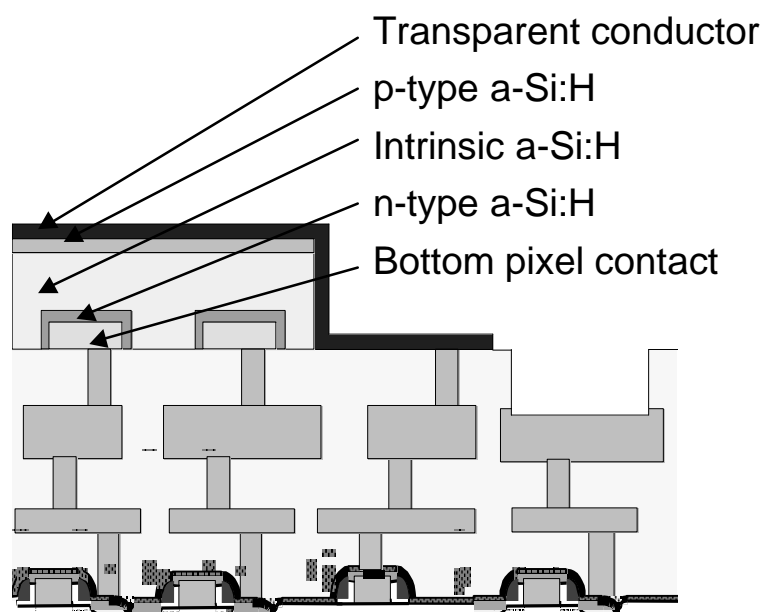


Figure 1: Drawing of elevated photodiode array cross-section.

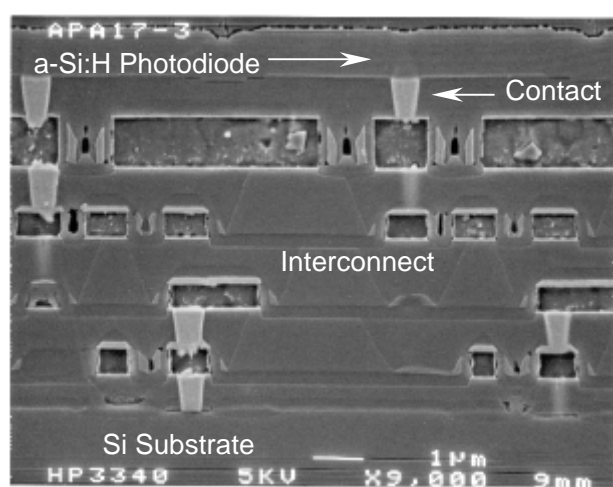


Figure 2: SEM cross section of elevated photodiode.

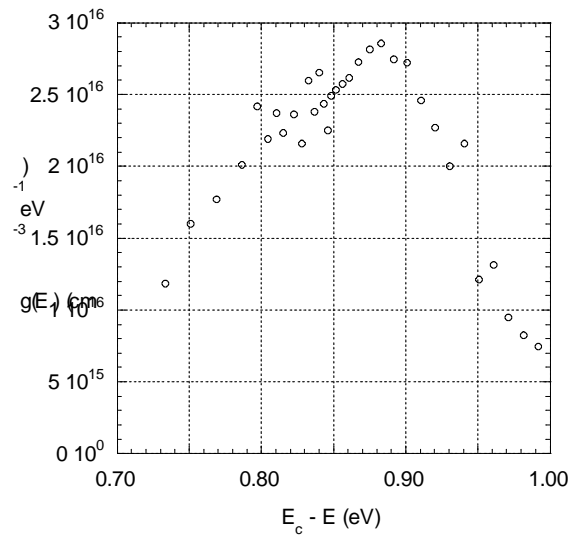


Figure 3: Deep-level density of states plot of a-Si:H used for these experiments.

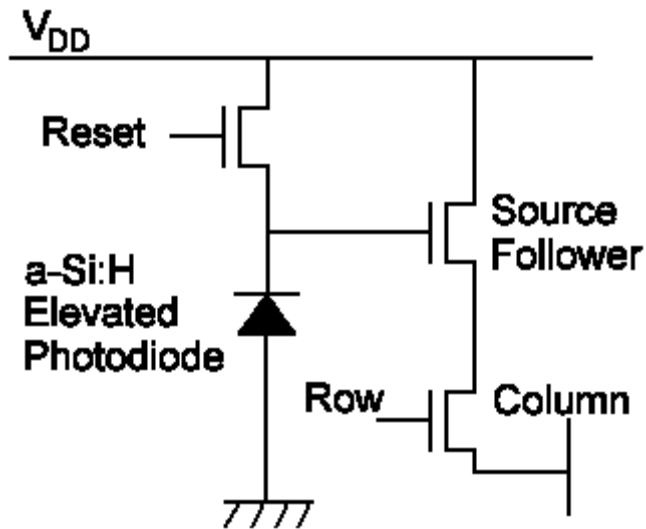


Figure 4: Pixel circuit schematic .

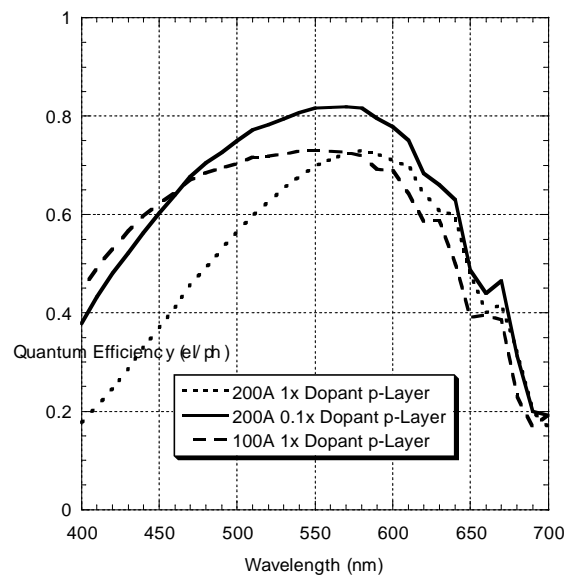


Figure 5: a-Si:H photodiode quantum efficiency collected under -2.5V bias.

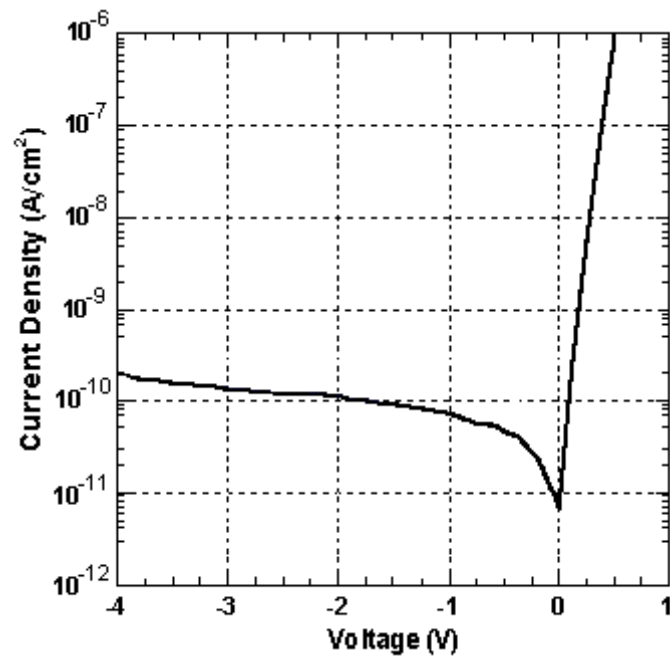


Figure 6: Dark current leakage as a function of applied bias.

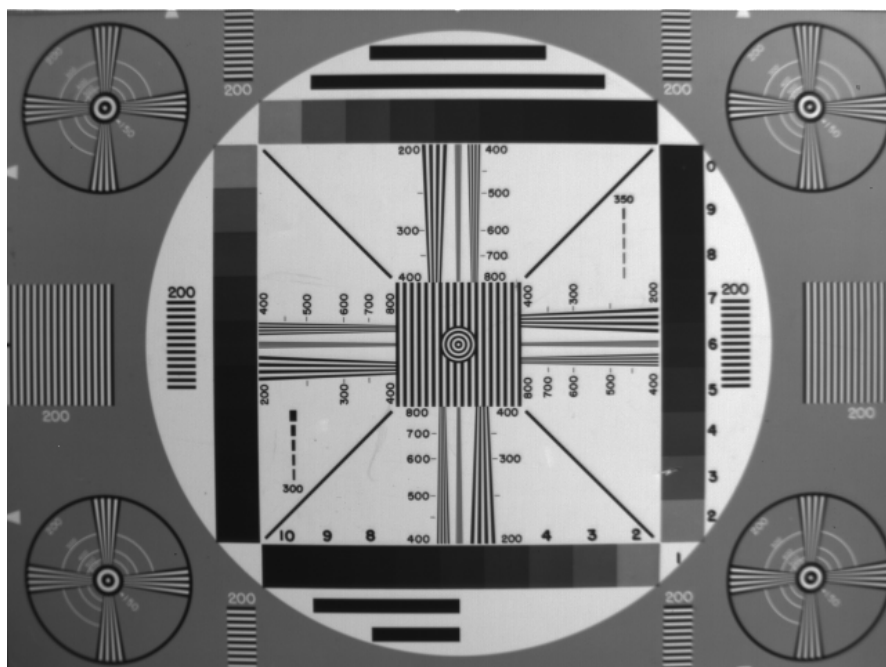


Figure 7: Test pattern image taken by a 10-bit VGA (640x480) a-Si:H photodiode array, with 5.9 μm by 5.9 μm pixels and 0.35 μm CMOS process.