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a-Si:H photodiode technology for advanced CMOS active pixel sensor imagers

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Abstract

Hydrogenated amorphous silicon (a-Si:H) holds the promise of realizing three-dimensional semiconductor integrated circuits by placing the photodiode above the pixel control circuitry rather than in-plane with it. This has the obvious advantages of enabling large die-size reduction and higher light collection efficiency compared to standard crystalline silicon arrays. We have developed a photodiode array technology that is fully compatible with 0.35 μm CMOS process flows to produce image sensors arrays with 10-bit dynamic range that are 30% smaller than comparable standard crystalline silicon photodiodes. These sensors have 50% higher sensitivity, and two times lower dark current when compared to bulk silicon sensors of the same design. The various methods of interconnection of the diode to the array and their advantages will be presented. Diode leakage currents as low as 30 pA/cm^2 have been measured. The effect of doped layer thickness and concentration on quantum efficiency (as high as 80% around 560 nm), and the effect of a-Si:H defect concentration on diode performance will be discussed.

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1. Introduction

Active pixel sensors are an attractive alternative to CCD image sensors because of lower power consumption, random pixel access, and a higher degree of system integration, which often leads to reduced overall system costs [1]. Several advantages could be realized by elevating the photodiode above the substrate such as, resolution improvements, maximizing the light collection area, introduction of more efficient semiconductor layers, and minimizing absorption of light from intervening layers. Several attempts to create elevated photodiode arrays on CMOS and CCD technologies have been demonstrated based on hydrogenated amorphous silicon (a-Si:H) as the semiconductor [2–7]. However, acceptance has been slow due to potentially expensive manufacturing techniques such as low a-Si:H deposition rates, difficulty in maintaining clean junction interfaces, and complex upper contact schemes; and difficult to control pixel isolation integration schemes.

This paper discusses the design and performance of an elevated sensor technology utilizing hydrogenated a-Si:H photodiodes, which overcomes all

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of these concerns. The features of this technology include high a-Si:H deposition rates to permit cost-effective high volume manufacturing, contact with the top side of the diode is monolithic which is mechanically robust and minimizes fabrication complexity, and a process flow that allows for well-controlled isolation of the pixel contact layer. In addition, the performance of the diode exceeds the optical performance of c-Si reverse bias photodiodes. For example, the absolute quantum efficiency of the photodiodes about 85% in portions of the visible wavelength regime, and the leakage current from the diode can achieve 80 pA/cm^2.

2. Elevated diode array and fabrication

Fabrication of the sensor starts with standard integrated circuits. At the pointing the process when the circuit undergoes passivation dielectric deposition, the dielectric is planarized to provide a flat surface on which to construct the photodiodes. The array consists of n-type a-Si:H pixels overlapping a thin metallic pixel contacts with a common intrinsic and p-type a-Si:H layers that form an array of p–i–n photodiodes (see Fig. 1 and the drawing in Fig. 2). However, if desired, the process allows for the manufacture of an array with p-type pixel junctions, and a n-type common junction. Top contact to the array is made by using a transparent conductor layer that connects the top surface of the p-type a-Si:H layer to vias adjacent

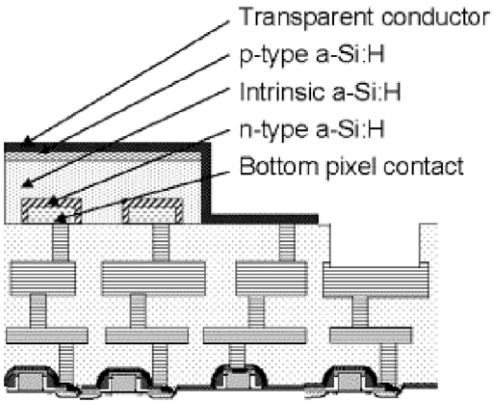

Fig. 1. Drawing of elevated photodiode array cross-section.

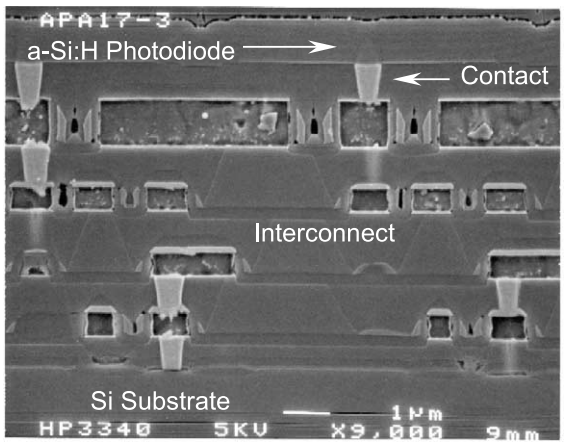

Fig. 2. SEM cross-section of elevated photodiode.

to the array (monolithic top contact structure) [8]. The a-Si:H pixels are patterned by photolithographic and etch steps to ensure adequate pixel isolation. The n-type a-Si:H overlaps the bottom contact pixel metal on all sides to minimize current injection. The pixel metal makes contact to standard via plugs that go through the upper isolation layer. It should be noted that while the transparent conductor is in direct contact with the intrinsic layer, current injection has not affected imager performance. The a-Si:H layers are formed by very high rate film deposition methods (> 30 Å/s), and the intrinsic layer is about 9000 Å thick. The a-Si:H used for this sensor has an intrinsic defect density of $< 6 \times 10^{15}$ cm^{-3} [9].

There are several methods by which contact can be made to the transparent conductor on top of the diode stack, both monolithic and external contact. The monolithic top contact structure was selected because of its low-cost and inherent high reliability (see Figs. 1 and 2). Other monolithic approaches include isolated strapping, which requires two additional masking steps and a highly selective contact etch. Alternative connection techniques involve using non-monolithic interconnections, such as wirebonding the transparent conductor to die-based or package-based bond pads. This would require wirebonding onto the transparent conductor, about which little is known for high volume integrated circuit packaging, and

may impose unreasonable stresses on the a-Si:H layers. Use of mechanical clips to the transparent conductor was also considered. However, this approach suffers from deficiencies in mechanical reliability with respect to packaging and electrical integrity of the contacts.

Allowing the transparent conductor to be in contact with the edge of the intrinsic layer for the array reduces the mask count by two with respect to the isolated strapping approach. This is a key point as the two mask reduction can reduce the cost of the array fabrication by 33%. The only concern is that the contact produces a forward biased junction that injects a dark current into the array. However, this arrangement does not degrade imager, since a high resistance can be inserted between the interface and the array, and any excess current can be drawn off by peripheral diodes in the array.

The contacting method to both the pixels and the common electrode utilizes standard metal vias. Via technology has advanced along with CMOS process development, so it is possible to create satisfactory vias with 0.5 μm diameter. It is important that the via take up a small area relative to the pixel size to ensure minimal spacing of circuit elements below. Direct contact require tapered vias, (to alleviate step coverage concerns) through the interconnect dielectric and could easily take up 20% of a 6×6 μm^2 pixel [6,7]. A standard CMOS via is made using an essentially vertical-walled cavity filled with W or Cu with a diameter of 0.5 μm. Such vias would take up less than 0.7% of the same pixel area, thus leaving the rest of the pixel area for circuit layout.

Fig. 3 shows the density of deep-level defects within the intrinsic layer. These measurements were carried out by the depletion transient current measurements as described in the work of Theil et al. [9]. Electron-spin resonance of the films show that the dangling bond defect density is between 2.5 and 4×10^{15} cm^{-3} which is considered state of the art. The hydrogen content of the films is about $14 \pm 2\%$ as measured by infrared spectroscopy.

3. Diode performance

The quantum efficiency for an a-Si:H photodiode across the visible spectrum is shown in Fig. 5. The efficiency ranges from 40% in the blue (400 nm) to almost 85% at 550 nm, and down to 15% at 700 nm. By comparison, bulk c-Si diodes have an efficiency across this range around 10–25%. Factors that lead to higher efficiency include 100% light collecting area across the pixel and a band gap of 1.85 eV for a-Si:H, which is more suited for collecting visible light than for c-Si. Fig. 5 also

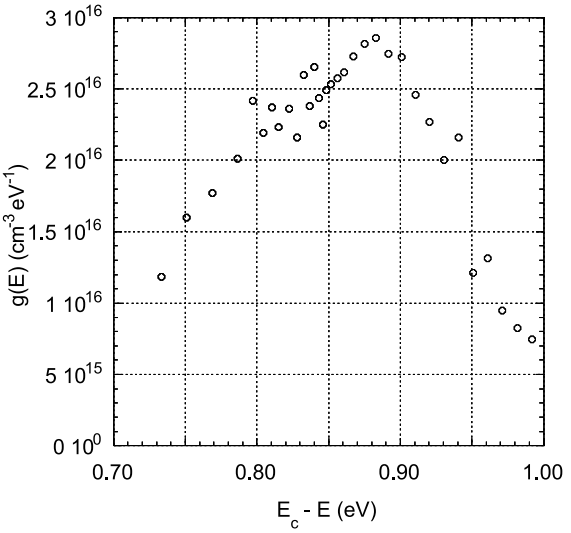

Fig. 3. Deep-level density of states plot of a-Si:H used for these experiments.

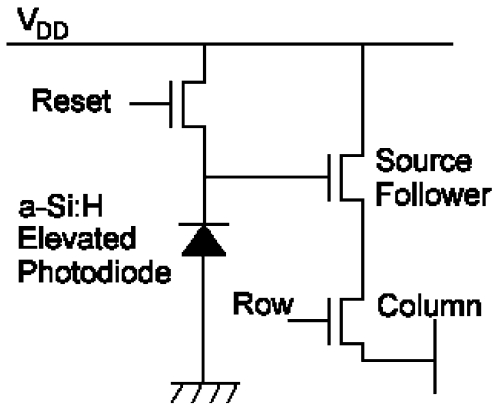

Fig. 4. Pixel circuit schematic.

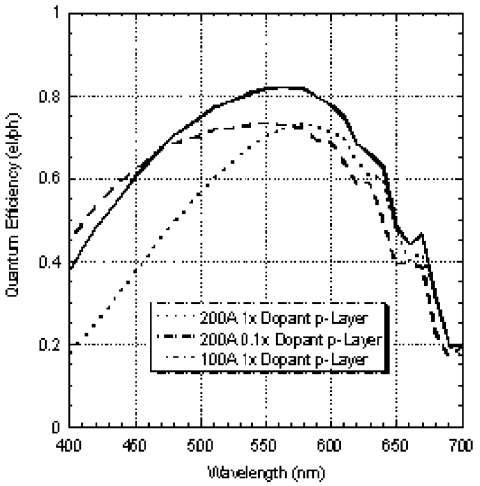

Fig. 5. a-Si:H photodiode quantum efficiency collected under −2.5 V bias.

shows that control of the upper doped contact layer controls the light collection efficiency of the shorter wavelengths. Minimizing the thickness of the p-layer and the dopant concentration of the p-layer maximizes the short-wavelength efficiency as shown in Fig. 5, as it allows the minimization of the depletion layer to the top surface of the diode. It is possible to increase the blue response at 400 nm from 20% to 40% across this range. Higher efficiencies could be achieved by thinning the i-layer, but this would be at the expense of red efficiency, which is limited by the absorption coefficient.

The intimate contact between the edge of the transparent conductor and the array creates an additional current component in the device. This current component can be eliminated by using a guard ring around the periphery of the diode to be measured. Because of current injected at the edge of the intrinsic layer, a guard ring structure was developed to separate the two current components. Fig. 6(a) shows the layout of the device measured. This structure has a 460×460 μm^2 area diode (denoted as Center Contact) surrounded, and a 10 μm wide guard ring entirely surrounding it. The outer most ring is a series of contacts to connect to the transparent conductor. An IV sweep was made by connecting the three terminals to separate source measurement units (SMUs) of a HP4145B and sweeping the bias of the guard ring and center contact with identical potentials from 0 to 10 V reverse bias. By holding the guard ring at the same potential of the structure of interest, it is possible to eliminate leakage currents from the ring to the inner device and at the same time prevent the edge intrinsic leakage current from reaching the inner device.

The electrical behavior of the diode is described by the IV curve shown in Fig. 6. The reverse bias curve shown in Fig. 6(b) shows the current density

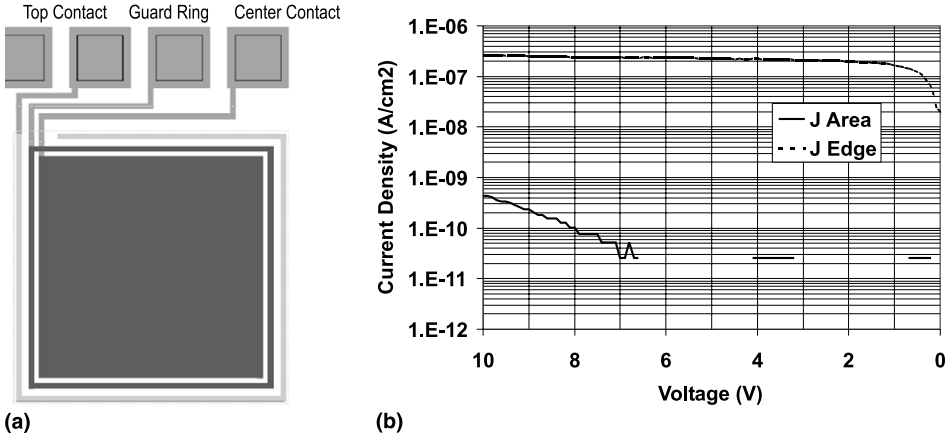

Fig. 6. (a) Test structure to measure dark leakage currents. (b) Dark current leakage as a function of applied reverse bias.

calculated from the two current components. It shows that the edge current density is a few orders of magnitude higher than that of the junction leakage, and that the junction leakage current density 30 pA/cm^2 at 7 V reverse bias. The leakage currents are low enough that our largest guard ring device could not detect the current at the operating voltages of interest. However, the work of Schiff et al. [10] shows that reverse bias central current shows exponential behavior down to below 1 V. Therefore, it is reasonable to estimate the leakage of the junction at 2.5 V by extrapolation, the leakage current density is about 2 pA/cm^2. However, work is continuing to developing devices capable of detecting lower current densities.

4. Sensor performance

The pixel circuitry for the array is a source follower circuit as shown in Fig. 4. It utilizes three NMOS FETs in a 4.9 μm square pixel, one as a reset, one as a row readout, and one as the source follower. The interpixel spacing is 1 μm. The source follower circuit is the smallest circuit that provides good signal isolation. Reference provides more details of a similar source-follower pixel circuit and its operation for c-Si sensor arrays [11]. The photosensor is compatible a mixed signal CMOS technology and has been implemented with a 0.35 μm process subtractive aluminum process. Devices using 4.9 μm square pixels have also been fabricated and provide similar performance.

Fig. 7 shows a test pattern image taken by a 10-bit VGA elevated photodiode imager. No evidence of fixed pattern noise, or point defects can be seen. Also, no interpixel leakage as manifested by blurred edges has been detected.

5. Summary

An elevated a-Si:H photodiode array with a reliable upper electrode contact has been realized

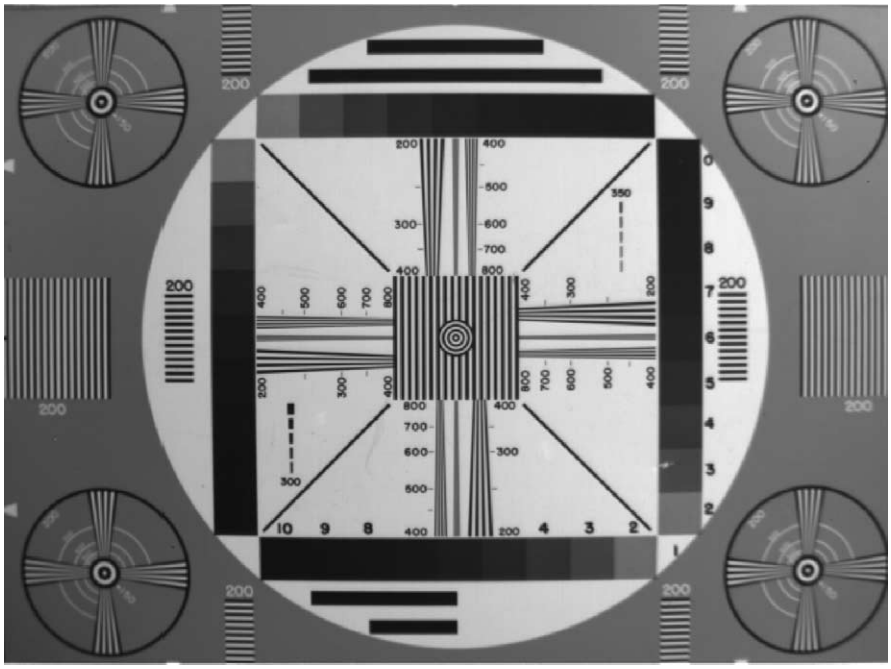

Fig. 7. Test pattern image taken by a 10-bit VGA (640 × 480) a-Si:H photodiode array, with 5.9 × 5.9 μm^2 pixels and 0.35 μm CMOS process.

in the form of a VGA imager. The CMOS-compatible sensor technology utilizes three key features, a transparent conductor strapping design that connects the common array electrode and vias with a number of minimum of masks, an etched n-type a-Si:H pixel layer, and high quality a-Si:H deposited with a high deposition rate. Quantum efficiencies of up to 85%, and leakage current densities of 30 pA/cm^2 at 7 V were measured, are obtained with diodes of this design. It is estimated that the current density may be as low as 2 pA/cm^2 at 2.5 V. While a working device has been demonstrated to perform in 0.35 μm CMOS, the technology is readily extendable down to the most aggressive dimensions available. The process also is compatible with color filter processing to allow creation of color sensor arrays. In summary, it has been shown that it is possible to couple elevated a-Si:H sensor arrays to standard CMOS processes and produce sensors that are at least equivalent to bulk silicon sensors.

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