FORMATION OF MULTILAYER SiO_2 - SiO_x HETEROSTRUCTURES BY CONTROL OF REACTION PATHWAYS IN REMOTE PECVD

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ABSTRACT

We have deposited thin films of silicon dioxide, SiO_2, and amorphous silicon, a-Si, by remote Plasma-Enhanced Chemical-Vapor Deposition (Remote PECVD), and have extended this process to the deposition of silicon suboxides, SiO_x, $0<x<2$. Heterostructures, comprised of alternating layers of SiO_2, and SiO_x, $x\sim1$, have been deposited by electronically controlling the flow of charged particles from the plasma-generation region into the deposition chamber, without interrupting the flow of process gases. We discuss the electrical properties of these heterojunction structures.

INTRODUCTION

We are engaged in a study of the deposition of Si-based electronic materials by low-temperature ($T_s<500°C$) Remote PECVD, and have identified the reaction pathways for the deposition of stoichiometric, and hydrogen-free SiO_2, and hydrogenated amorphous silicon, a-Si:H [1,2]. We have studied the electronic properties of the deposited films, and have evaluated their performance in device structures [3]. In this paper we demonstrate: i) the extension of Remote PECVD to the formation of silicon suboxides with controlled Si:O ratios; ii) deposition of multilayer heterostructures of SiO_2, and SiO_x, $x\sim1$, by Remote PECVD by simply controlling the bias to a grid electrode in the deposition system; and iii) multilayer device structures.

REACTION CHEMISTRY

Deposition of silicon suboxides by Remote PECVD results from two independent reactions occurring simultaneously. The first produces an a-Si:H alloy component, introducing Si-Si and Si-H bonds into the suboxide; and the second produces an SiO_2 alloy component, introducing Si-O-Si bonding groups. The deposition of a-Si:H, and SiO_2 by Remote PECVD can be accomplished by the following two reactions [1,2]:

$$\{He\}^* + SiH_4 \text{ ---> a-Si:H, and} \quad (1)$$

$$\{O_2 + He\}^* + SiH_4 \text{ ---> } SiO_2, \quad (2)$$

where the starred brackets enclosed the plasma excited species. SiH_4 is introduced downstream from the plasma excitation region to prevent direct plasma-excitation and fragmentation. A portion of the Deposition/Analysis system, used to study reaction pathways, and also used for the deposition of the oxide and suboxide films used in this study, is shown in Fig. 1. Ar diluted silane (10% SiH_4/90% Ar) is introduced, at a flow rate of 10 sccm, via a gas dispersal ring, located "downstream" from the plasma generation region A He/O_2 mixture (500:1), at a flow rate of ~100 sccm is plasma excited, and then transported into the deposition region where the process pressure is maintained at 300 mTorr. These conditions of gas flow and process pressure prevent any back-streaming of silane into the plasma generation region.

The important feature of this chamber is the plasma bias assembly, located immediately downstream from the plasma generation region. The extent to which the plasma afterglow extends downstream from this assembly depends on the bias state

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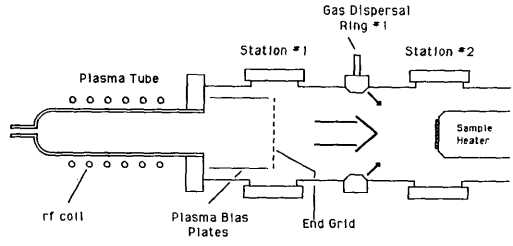

Fig. 1. Section of Deposition/Analysis system showing plasma-excitation region, grid-bias assembly, down-stream gas-dispersal rings, and ports for process diagnostics, Mass Spectrometry and Optical Emission Spectroscopy.

[1,2]. When the plates of grid are electrically floating, the afterglow does not extend beyond the end grid; when the grid is grounded, the afterglow extends downstream into the region of the chamber in which the silane is introduced. The deposition of a-Si:H occurs when the grid is grounded and the He plasma afterglow, primarily electrons that result either from the plasma excitation process, or from recombination of He metastables, activate the silane. Studies based on mass spectrometry, have shown that the activated silane is not fragmented prior to the actual deposition reaction [1,2]. No a-Si:H deposition occurs if the grid is in the floating state [1,2]. He metastable species, produced in He plasma discharge, do not play a significant role in this deposition process for a-Si:H because their flow through the grid assembly is not changed by the bias state of the grid.

For the deposition of SiO_2, a He/O_2 mixture flows through the plasma tube and is subjected to plasma excitation. Stoichiometric SiO_2 has been produced for all concentrations of O_2 in He, from pure O_2 to as low as 0.1% O_2 in He. This occurs when the end grid is in the floating condition so that the plasma afterglow does not extend into the deposition region. Under this condition of grid bias, the silane reactant is not plasma activated. With a SiH_4/Ar flow of 10 sccm, the ratios of SiH_4 to O_2 which have been investigated range from 10 to 0.01, a factor of 10^3. Other experiments have shown that the active oxygen species is neutral, e.g., the molecular metastable, O_2^* [1]. Eqn. (3) describes the complete deposition reaction for the formation of SiO_2,

$$O_2^* + SiH_4 \text{ --> } SiO_2(s) + H_2(g) + H_2O(g), \qquad (3)$$

where the O_2^* is generated by plasma excitation. The relative concentrations of the by-products, $H_2(g)$ & $H_2O(g)$, depend of the relative flow rates of O_2 + SiH_4, with H_2 being dominant for O_2 « SiH_4, and H_2O being dominant for O_2 » SiH_4 [1,2].

Suboxides have been deposited under the following conditions: i) an SiH_4/O_2 ratio is » 1.0: for a 0.1SiH_4/0.9Ar flow of 10 sccm, the concentration of O_2 in He with a flow rate of 100 sccm, must be much less than 1.0 %; and ii) the end grid in the grounded bias state so the plasma afterglow extends in the deposition region. If the concentration of O_2 is > 1.0%, then two factors limit the formation of suboxides: i) the relative deposition rates for the a-Si:H and SiO_2 alloy components; and ii) the suppression of He metastable production by the O_2 source gas. In this study, we have adjusted process gas flow rates, plasma power, etc., so that SiO_2-SiO_x multilayer structures can be deposited by changing only one condition - the bias state of the end grid between the plasma excitation region and the deposition region. This is done without adjusting, switching, or interrupting either the gas flows, or the rf power.

SAMPLE PREPARATION AND MEASUREMENTS

Thin film structures, comprised of Remote PECVD SiO_2 and SiO_x layers were deposited at 300°C, at an RF power of ~30 Watts, and onto crystalline silicon (c-Si) substrates, prepared by a modified RCA-clean process [3] just prior to inserting them into the deposition system load-lock. For the TEM analysis and IR studies, we used a (100) p-type 30-60 Ω cm substrate; for the electrical measurements we used (111) oriented n-type epitaxial wafers with a resistivity of 5 Ω cm in the 15 μm thick epi-region. The IR studies indicated a Si-O bond-stretching absorption band that shifted monotonically with changing Si:O ratios; this establishes that the deposited suboxides are homogeneous alloys, rather than mixtures of a-Si and SiO_2. Aluminum dots having an area of 1.15×10^{-3} cm^2 are evaporated through a shadow mask onto the top side of the devices structures. Al was also use to contact the n+ Si backside of the epi-wafers. After metallization, the samples were annealed at 400 °C in flowing dry N_2 for 1 hr. High frequency (1 MHz) C-V measurements were carried out in the dark with a Model 410 Micromanipulator instrument.

TEM IMAGING

A sample was prepared for TEM imaging by first depositing a thin layer of SiO_2 (layer A) onto the c-Si substrate. Without interrupting gas flow or changing any other deposition parameters, the grid was switched to ground and a thicker SiO_x, x~1, suboxide layer (layer B) was deposited. A second SiO_2 layer was then deposited by switching the grid back to the floating condition. This sequence was repeated until five "A,B" pairs were deposited with a final SiO_2 capping the multilayer structure. Figure 2 show a bright-field TEM image taken on a Hitachi H-800 instrument using 200 KeV primary electrons at a magnification of 100K. The atomically-denser suboxide layers show up as dark bands, and the oxide layers as lighter bands. The initial SiO_2 layer is about 79 Å thick, and the subsequent SiO_2 layers are thinner, approximately 52 Å,even though the same deposition times were employed. The SiO_1 suboxide layers are all about 145 Å thick. The estimated error in thickness determinations is ±13 Å. The micrograph confirms that the suboxide is a homogeneous alloy of Si and O, and not a two-phase mixture of a-Si and SiO_2. The micrograph also demonstrates that the metallurgical interface between the oxide and suboxide layers is less than ~15 Å. The differences in thickness between the first SiO_2 deposition onto the c-Si substrate, and the remaining SiO_2 layers deposited onto the suboxides, derive from a subcutaneous oxidation process [3-5], which can occur during film deposition. While the film deposits, atomic oxygen, also a by-product of plasma excitation can migrate through the oxide, and initiate low temperature oxidation of the c-Si substrate. The difference in thickness is consistent with our determinations of the self-limiting oxide growth under the conditions of Remote PECVD deposition used. There is no evidence for a similar subcutaneous oxidation process occurring at the interface between suboxides and the Remote PECVD deposited oxides.

CAPACITANCE-VOLTAGE (C-V) MEASUREMENTS

Several different samples were prepared for C-V measurements. Sample M04 is a metal-oxide-semiconductor (MOS) structure with a single layer of oxide,which serves as a benchmark for evaluating the electrical quality of the deposited oxide layers. C-V data are shown in Fig. 3, where the trace, from +5 V to -5 V, and the retrace are essentially overlapping. The scan speed is 10 V/s and a delay period of 1 ms occurs before beginning the retrace. Subsequent scans show that these traces shift apart in the negative voltage direction, indicating a slow buildup of positive oxide charge, possibly from ions originating at the oxide-metal gate electrode interface.

To investigate the potential of the suboxide layers for charge storage, three samples were made, each consisting of three deposited layers: i) an initial thin oxide layer deposited onto the c-Si substrate (20Å, 40Å and 84Å for three structures); ii) a suboxide, ~150Å; and finally iii) a thicker oxide, ~165Å. The thickness of the first oxide layer was varied to control tunnel injection from the Si-substrate into the suboxide, and from the suboxide back into the Si-substrate. The second oxide layer was sufficiently thick to prevent tunneling from either the suboxide into the metal gate electrode, or in the reverse direction.

The C-V data for these three heterostructures are shown in Figs. 4, 5 and 6. The C-V curves in Fig. 4, for the device with the 84Å SiO_2 layer thickness, are similar to those in Fig. 3, and do not show any measurable injection of electrons from the c-Si substrate, through the 84Å, and into the SiO_1 suboxide layer. For the samples having thinner initial oxide layers, the C-V data in Figs. 5 (40Å oxide) and 6 (20Å oxide) show that electrons have tunneled into the suboxide layer as evidenced by the positive shift (~ +4 V) in the flat-band voltage of the initial traces. Before initiating a trace, the gate voltage (V_G) was held at +5 V for about 5 minutes, to ensure that the amount of negative charge that had tunneled into the suboxide was the same before each scan was made. This is confirmed by the flat-band shifts of just under 4V for all of the initial traces in Figs. 5 and 6.

As V_G swings negative during the initial trace, electrons can tunnel back out of the suboxide into the silicon substrate. Figs. 5 and 6 show the effect of different delay times between the end of the initial trace and the beginning of a particular delayed retrace. This allows us to investigate the time dependence of any discharging mechanism by maintaining a V_G of -5 V at the end of a given initial trace for different time delays. The scan speeds for the trace and retrace curves are the same, 10 V/s, so that discharging effects at times longer than about 0.5 to 1 second can be investigated.

As the delay time increases from 0.1 s to 500 s for sample with the 40Å oxide, retrace curves are displaced in the positive voltage direction, with the flat-band voltage approaching ~0.0 V as the delay time increases to 500 s. For shorter delay times, the flat-band voltages are more positive (>0.0 V), and decrease in magnitude with increasing delay time. These delayed retraces indicate that most of the electrons, originally injected into the suboxide, have tunnelled back out of the suboxide during the 500 s delay period for which the gate voltage was held at -5 V. In contrast, even a time delay of as small as 0.1 s for the structure with 20Å oxide is sufficient for all of the electrons to leave the suboxide layer, and for the suboxide layer to take on a net positive charge as evidenced by the negative flat-band shift in Fig. 6.

ANALYSIS OF C-V DATA

The C-V data have been used to estimate a low frequency dielectric constant for the suboxide material. Figures 5 and 6 show that the maximum capacitance for the heterostructures with 40Å and 20Å oxides, are 135 pF and 149 pF, respectively. If the difference between these values is due entirely to the difference in the thickness of the thinner oxide layers, then we estimate that a static dielectric constant for the suboxide of about 6.9±0.3. Values in this range are expected, since they must fall approximately half-way between values of 11.7 for Si and 3.9 for SiO_2. As the O/Si ratio increases from zero, the optical band gap (E_G) increases. We have measured E_G , taken here as the photon energy, E_{04}, at which the absorption constant is 10^4 cm^{-1}; for suboxides having an O/Si ratio ~1.0, we find that E_G is about 2 eV [6], consistent with previously reported data for homogeneous suboxides [7].

The C-V data have also been used to study charging effects [8]. The initial traces for structures with 40Å and 20Å oxides, show the same positive shift (~ +4 V) in the respective C-V curves (see Figs. 5 and 6), indicating that with the application of the +5 V gate bias, about 3 x 10^{12} electrons/cm^2 have tunneled out of the Si-substrate, through the thin oxide, and into the suboxide layer where they have become trapped.

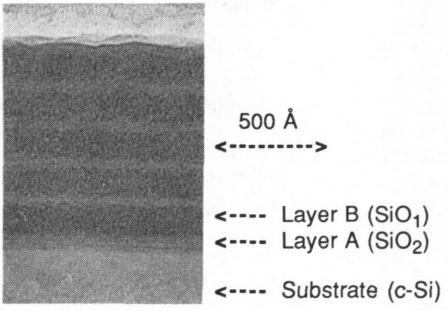

Fig. 2 TEM of multilayer structure: A is SiO_2 & B is $SiO_{1.0}$.

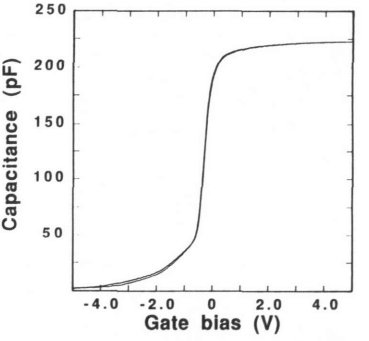

Fig. 3. C-V curves of MOS device. Scan speed is 10 V/s; delay time, 1 ms.

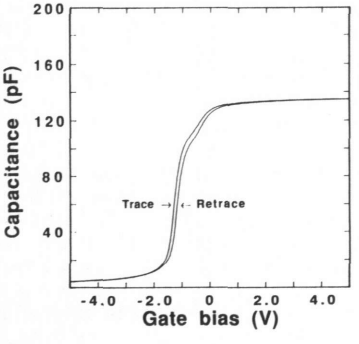

Fig. 4 C-V curves of device with 84Å oxide.

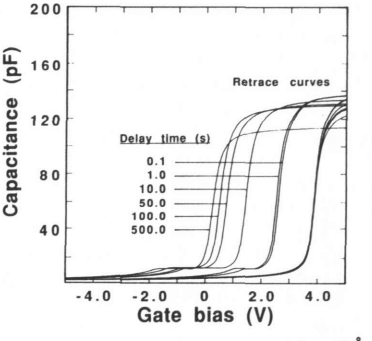

Fig. 5. C-V curves of device with 40Å oxide.

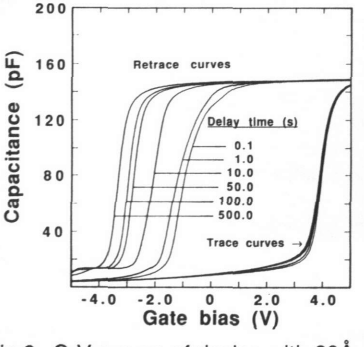

Fig 6. C-V curves of device with 20Å oxide.

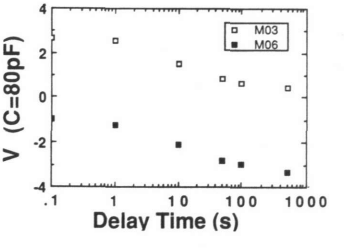

Fig. 7. V(C=80pF) versus delay time for devices with 20Å & 40Å oxides.

The data in Figs. 5 and 6 allow us to investigate the time-dependence of the discharge process. This is accomplished by sweeping rapidly from a V_G of +5 V to a V_G of -5 V during the trace scan, and then delaying for different periods of time before retracing rapidly back to a V_G of +5 V. By increasing the delay time at the fixed negative bias, the number of electrons extracted from the suboxide can also increase. Changes in the flat-band voltage, δV_{FB}, of the retrace are then used to monitor the amount of charge remaining trapped in the suboxide layer after a time-dependent partial discharge. Figure 7 shows the result of this analysis, where we plot the voltage at which the capacitance has risen to an arbitrarily chosen value value of 80 pF, V(C=80pF), vs the delay time, (the oxide thickness of sample MO3 is 40Å, and that of MO6 is 20Å). Both V(C=80pF) and δV_{FB} provide a direct measure of the relative discharge rates.

There are three things to note in Fig. 7. First, the time required to completely discharge the suboxide at a V_G of -5 V for the sample with an oxide thickness of 40 Å, is more than 1000 seconds. Second, by decreasing the oxide, or tunneling barrier thickness by a factor of two, as in the sample with an oxide thickness of 20Å, the structure completely discharges in a time of less than 0.1 seconds. Third, as the delay time increases beyond 0.1 seconds, the suboxide in the structure with the 20Å oxide becomes positively charged as indicated by the negative values for V(C=80pF).

Three requirements that must be satisfied for charge storage devices are: i) charge injection into a storage layer; ii) charge trapping in the storage layer; and iii) charge removal from the storage layer. The suboxide layer provides charge storage, and the thin and thick oxide layers control the flow of charge into, and out of the semiconductor substrate and the gate electrode ,respectively. Charge injection into, and charge removal from the suboxide, are accomplished by a direct tunneling process. Tunneling of electrons is possible for oxide thicknesses of 20Å and 40Å, but is not possible of a thickness of 84Å. Similar considerations apply for charge removal from the suboxide. The only difference between the 20Å and 40Å tunneling barriers relates to the fact that with the 20Å barrier electrons, beyond those injected into the suboxide can be extracted with a reverse bias. This means that the states which electrons tunnel into the suboxides are not the same states from which they are extracted. Positively charged suboxides have also been observed by other workers [9] and they are thought to be associated with the removal of electrons originating in donor-like states in the suboxide, rather than from hole injection into the suboxide.

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